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DMS-SA30

Rev.10

Intel Skylake-S

CPU:

Intel SKL-S CPU (LGA1151)
Max. TDP: 35W

System Chipset:

Intel 100 series
Q170/H110

Main Memory:

DDR4-1866/2133 SO-DIMM x2 (1DPC, Max:32GB)

On Board Chip:

HDMI to LVDS - TSUMU58DC2-1
eDP to VGA - CH7517A
Super I/O - NCT6106D
Audio - Realtek HD Audio Codec ALC898 + Amplifier TPA2008D2
LAN - Intel Jacksonville i219LM(Q170) / V(H110)
BIOS - SPI Flash ROM 128MB(Q170) / 64MB(H110)
TPM 2.0/1.2 - SLB9665/9660 (For Q170 SKU)
GL850G - USB2.0 HUB (For H110 SKU)

VRM Controller:

IMVP8-ISL95855(VCCP/VCCGT/VCCSA)
ISL8016(VCCIO)
NCP1589L(VCC_DDR) + UP1727(VPP_DDR)
NCP1589L(PCH_1VSB)
NCP1589A(+12VSB)
TPS40210DGQ(+24VSB)
TPS51125RGER(SYS_PWR)

Expansion Slots:

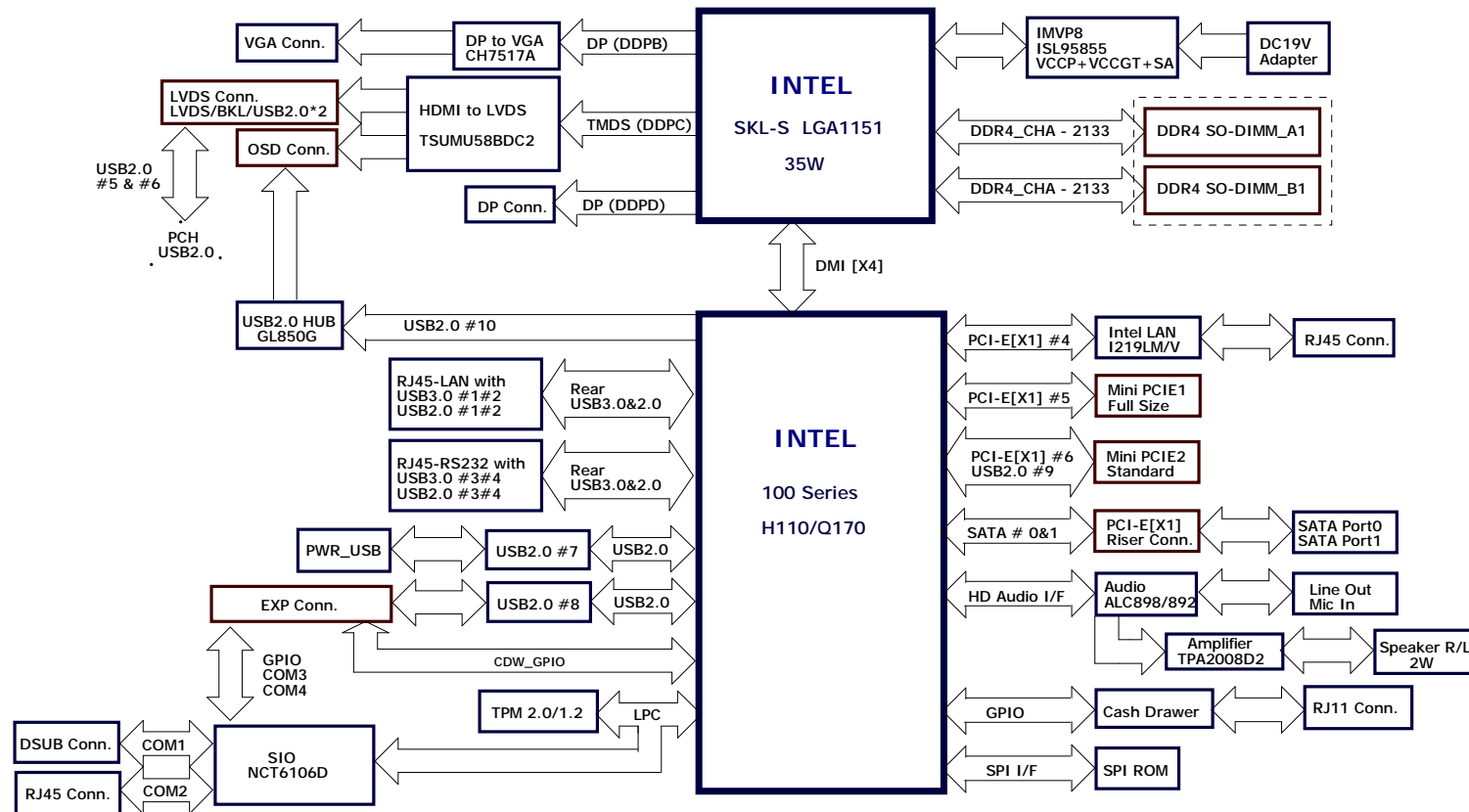
SATA Riser Connector (2* SATA ports)
Mini-PCIE *2
Expansion Board (RS232*2, USB*1 ...)

Others :

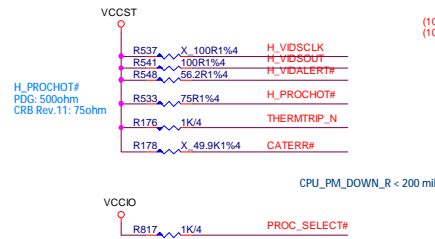
Cash Drawer
Power USB



Block Diagram

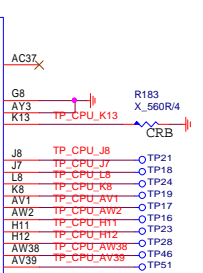
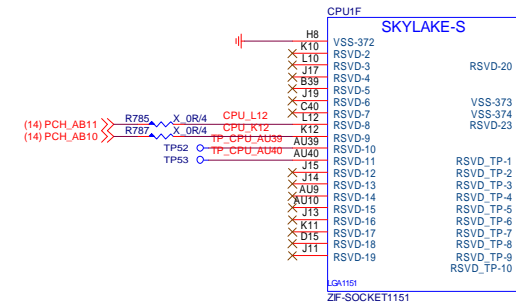
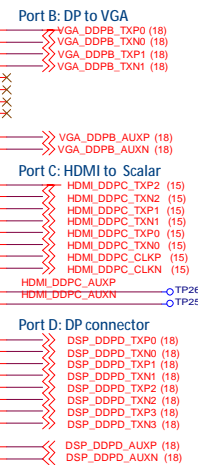
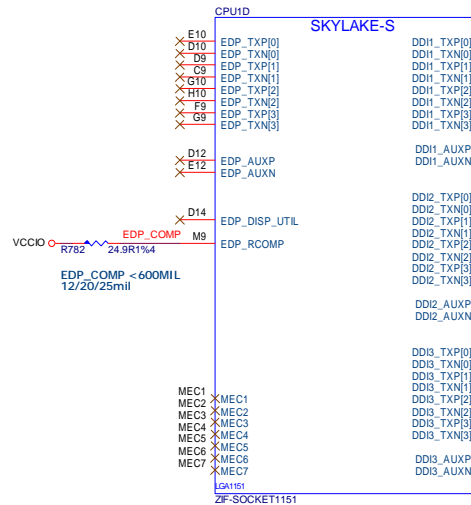
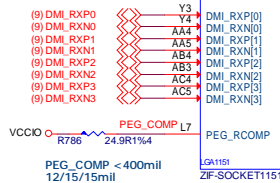
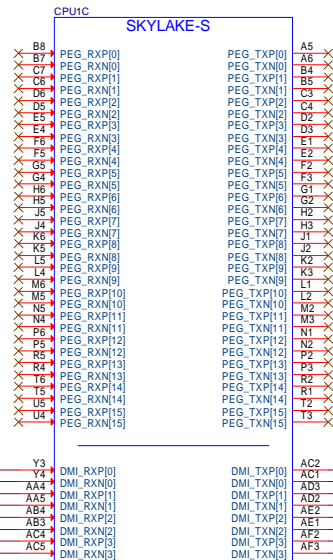
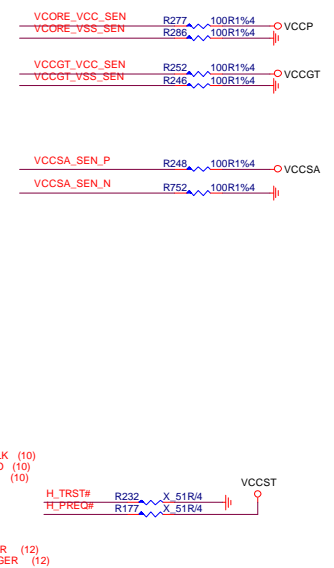
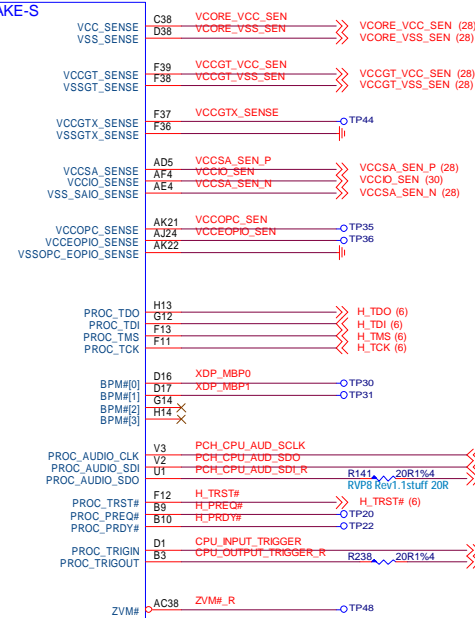
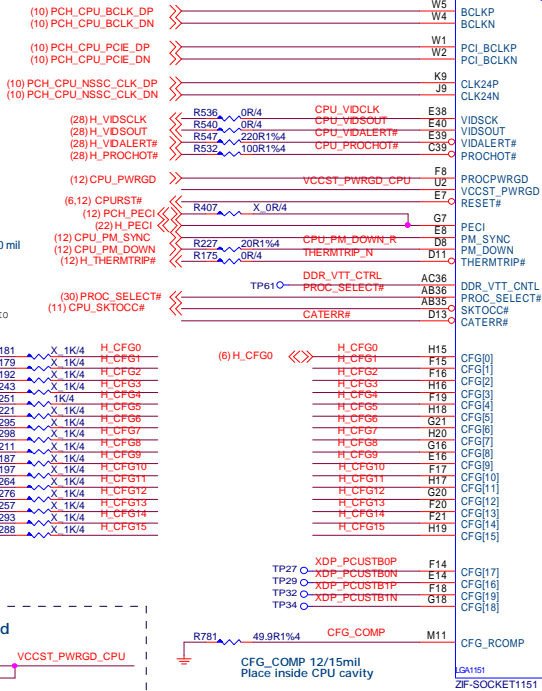
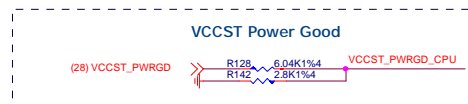


CPU-CTL/MISC/CFG/Audio/DSP

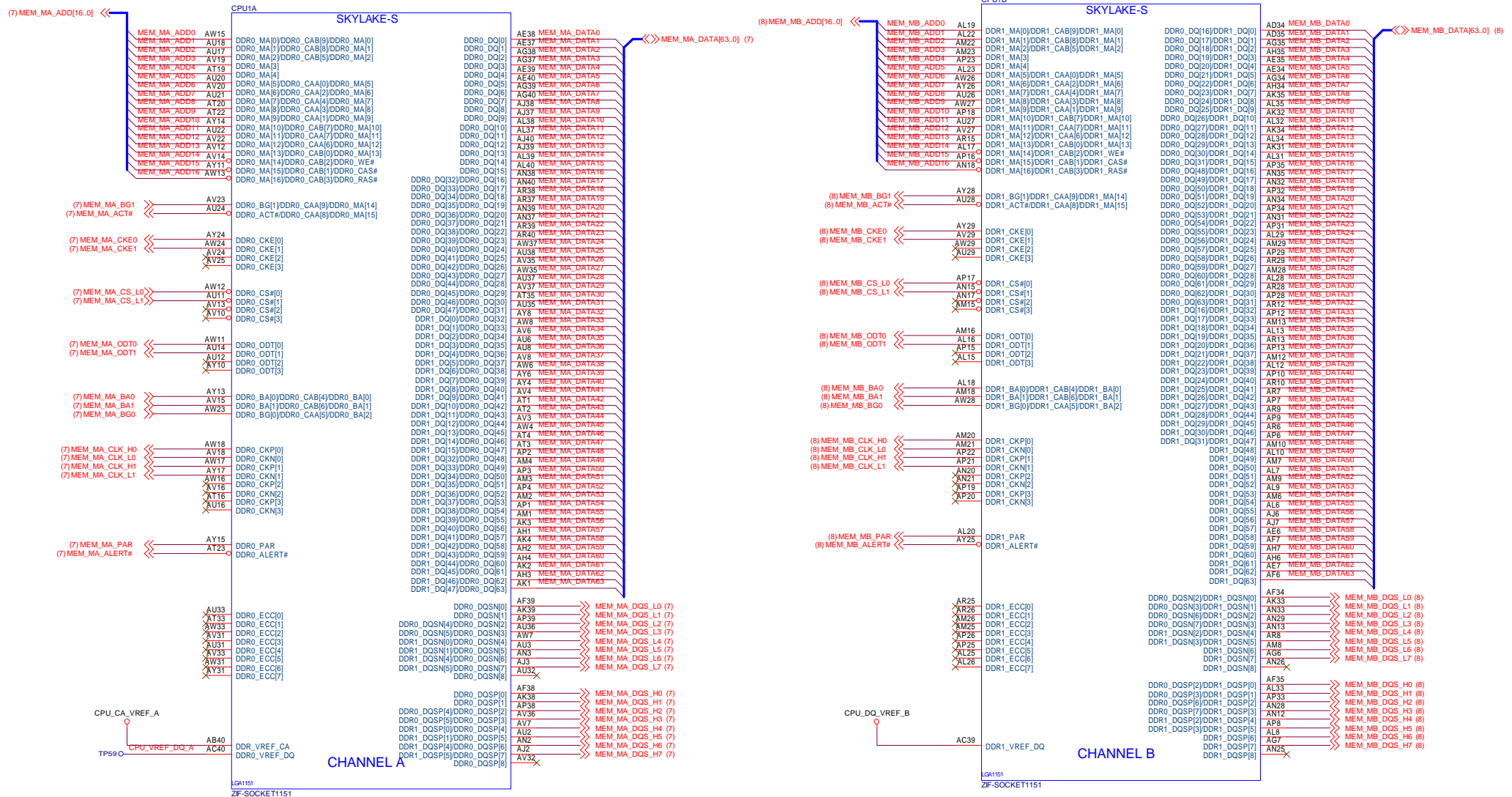


Processor Strapping
CFG[0] ITP will drive the net to GND.
CFG[2] Reserved. No connect
CFG[4] Display Port Presence strap
=1: Disabled - No Physical Display Port attached to Embedded DisplayPort* No connect for disable.
=0: Enabled - An external Display Port device is connected to the Embedded Display Port.
CFG[5,6] (1, 1) PCIe 16X
CFG[19:5] Reserved configuration lands
A test point be placed on the board for these lands

CRB1.0 Note
PD CFG9 FOR HASWELL INTERPOSE
PD CFG12 FOR HASWELL INTERPOS
PD CFG13 FOR LPT-H INTERPOSER

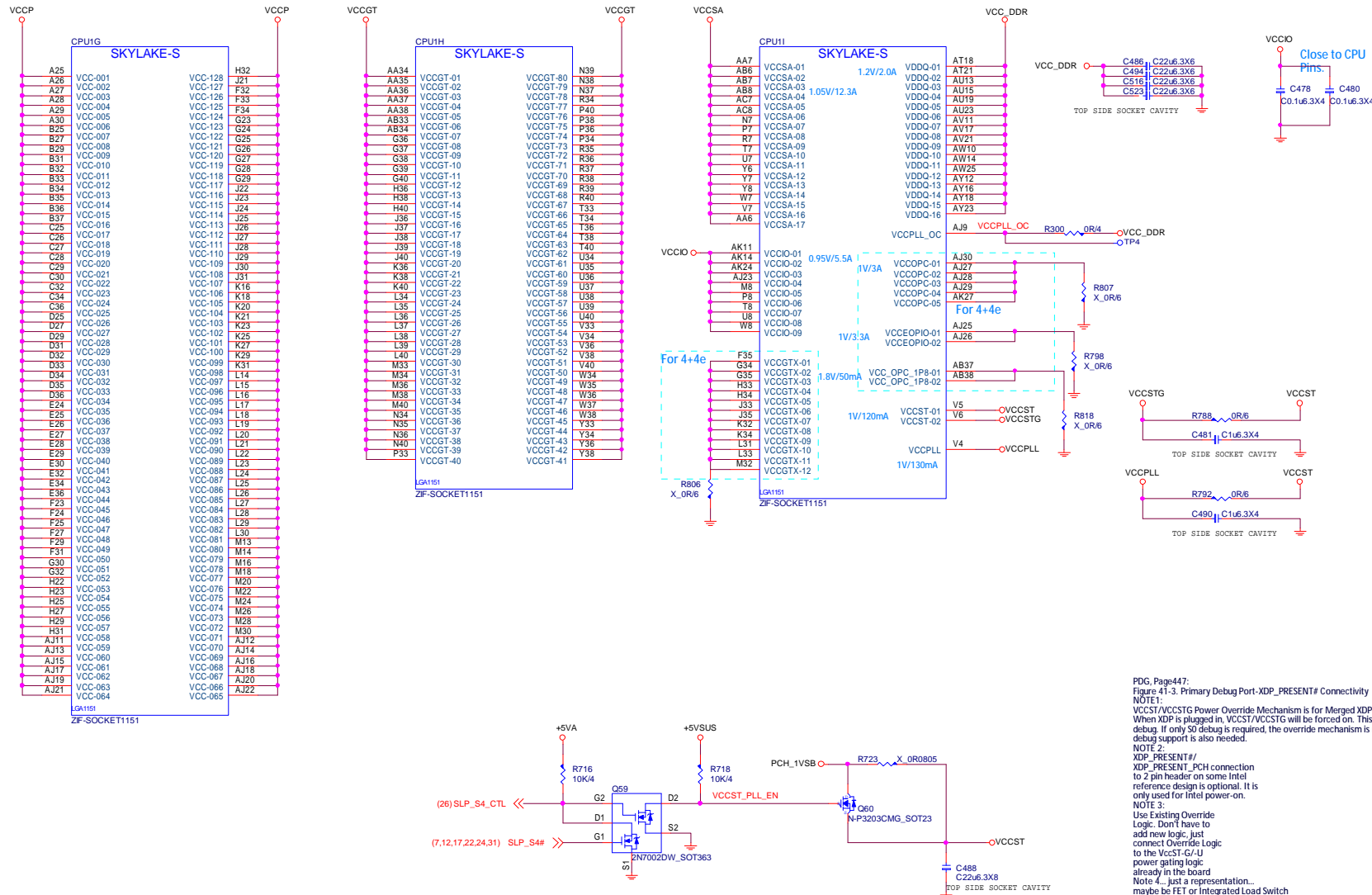


CPU-Memory



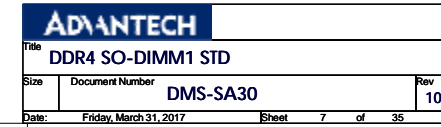
SOCKET PN N12-151A010-L06

CPU-Power



PDG, Page 447:
Figure 41-3. Primary Debug Port XDP_PRESENT# Connectivity
NOTE 1:
VCCST/VCCSTG Power Override Mechanism is for Merged XDP usage model.
When VCCST is plugged in, VCCST/VCCSTG must be forced on. This is to support PCH Sx
debug. If only S0 debug is required, the override mechanism is not required unless C10
debug support is also needed.
NOTE 2:
XDP_PRESENT#/XDP_PRESENT_PCH connection to 2 pin header on some Intel
reference design is optional. It is
only used for Intel power-on.
NOTE 3:
Use Existing Override
Logic. Don't have to
add new logic. Just
connect Override Logic
to the VccST-G/I-U
power gating logic
already in the board
Note 4. Just a representation...
maybe be FET or Integrated Load Switch

Channel A (W/O ECC)

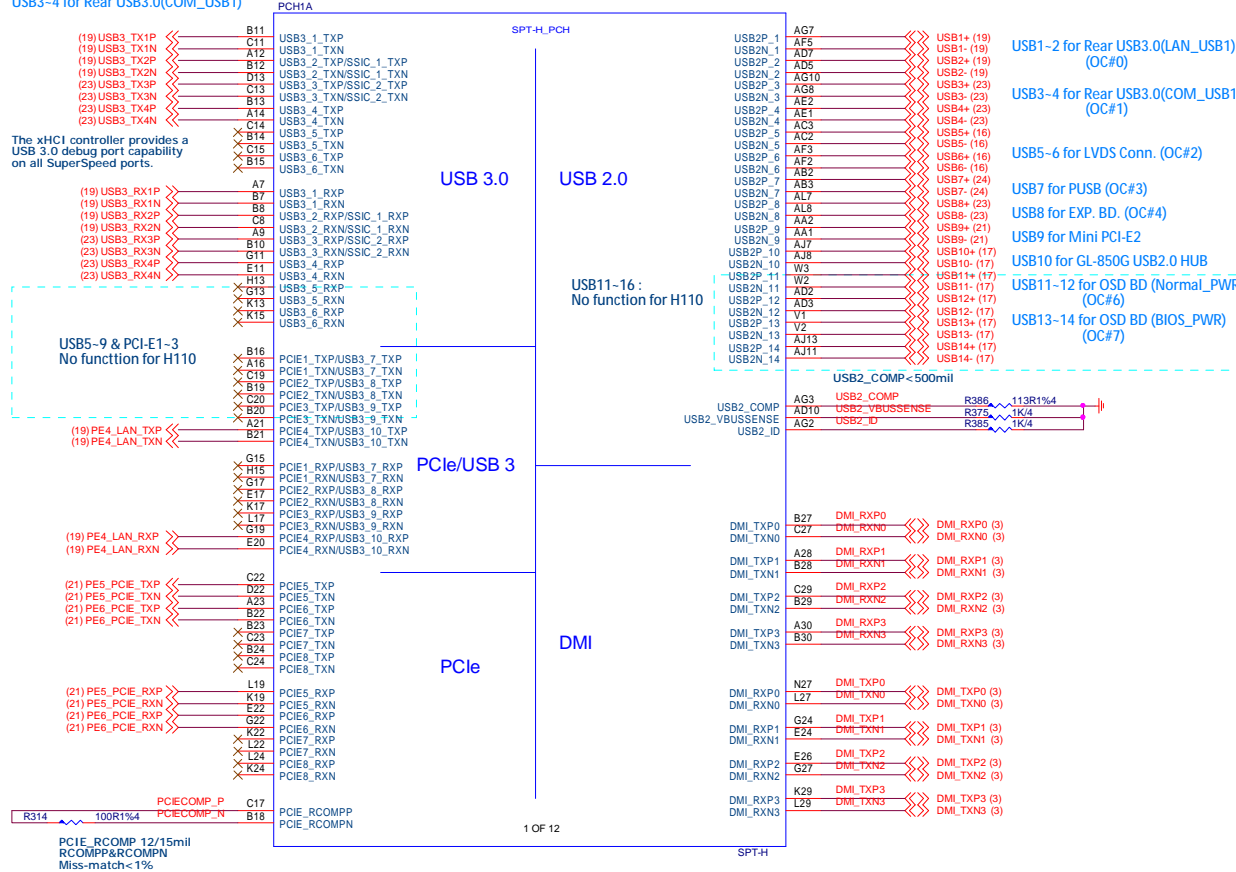


Channel B (W/O ECC)

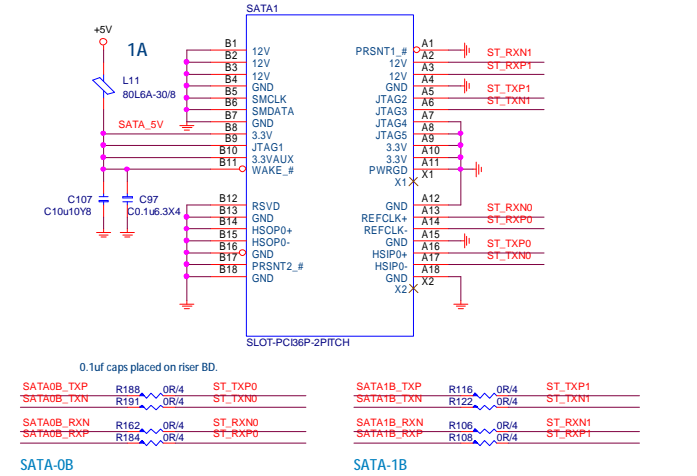


PCH-USB/PCIE/DMI/SATA

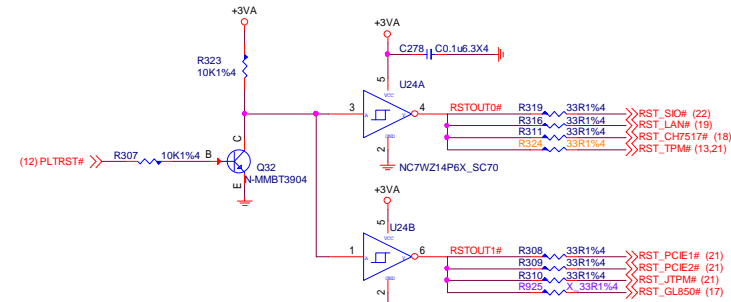
USB1~2 for Rear USB3.0(LAN_USB1)
USB3~4 for Rear USB3.0(COM_USB1)



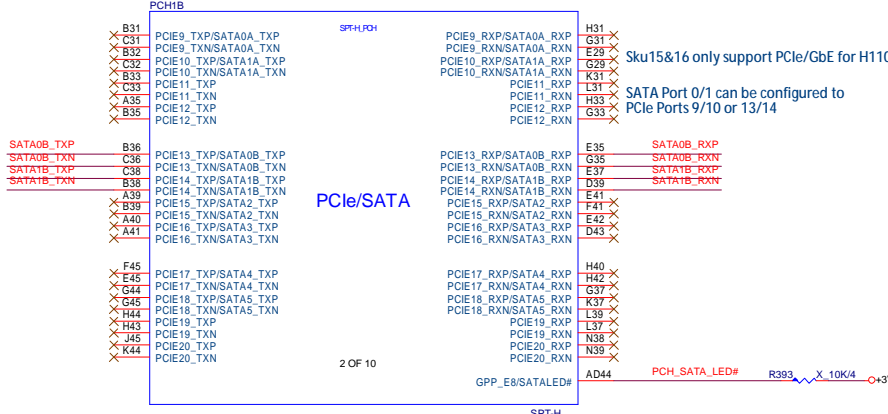
SATA Riser Connector



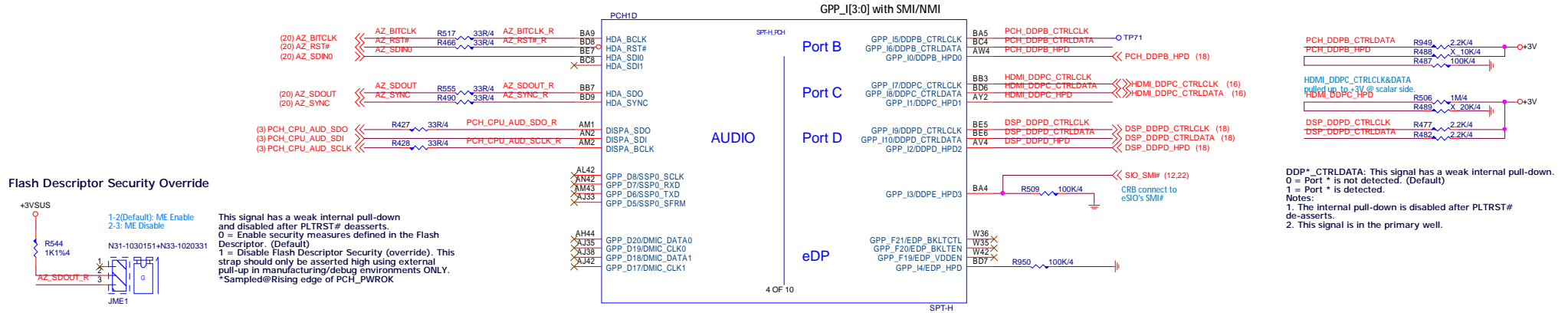
PLTRST# Buffer



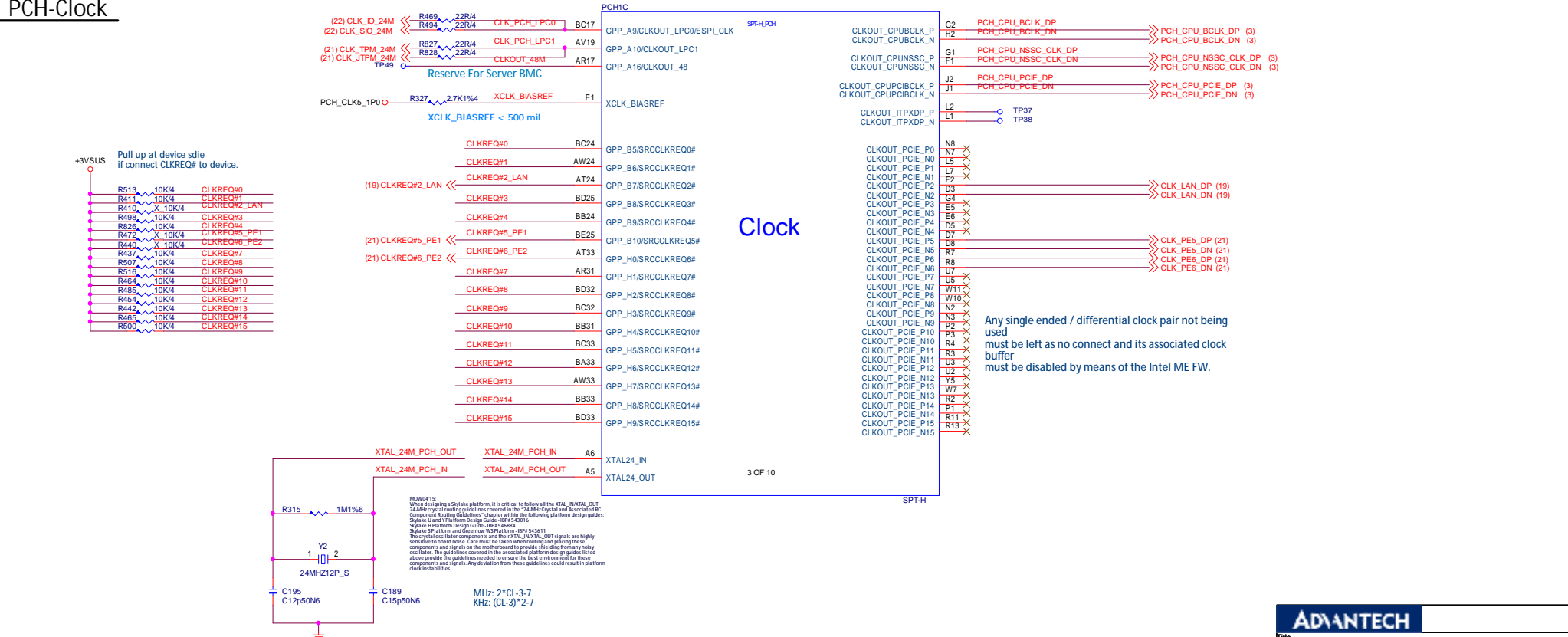
Lane11 of H110 is N/A and lane 12 only can be used for LAN only.



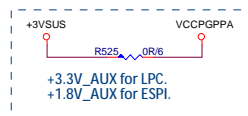
PCH-Audio & Display



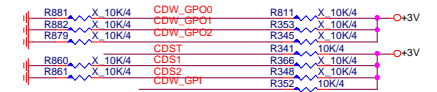
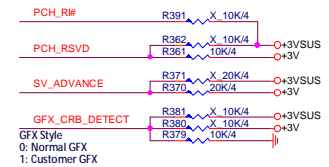
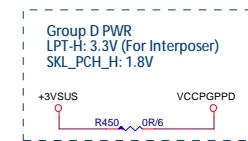
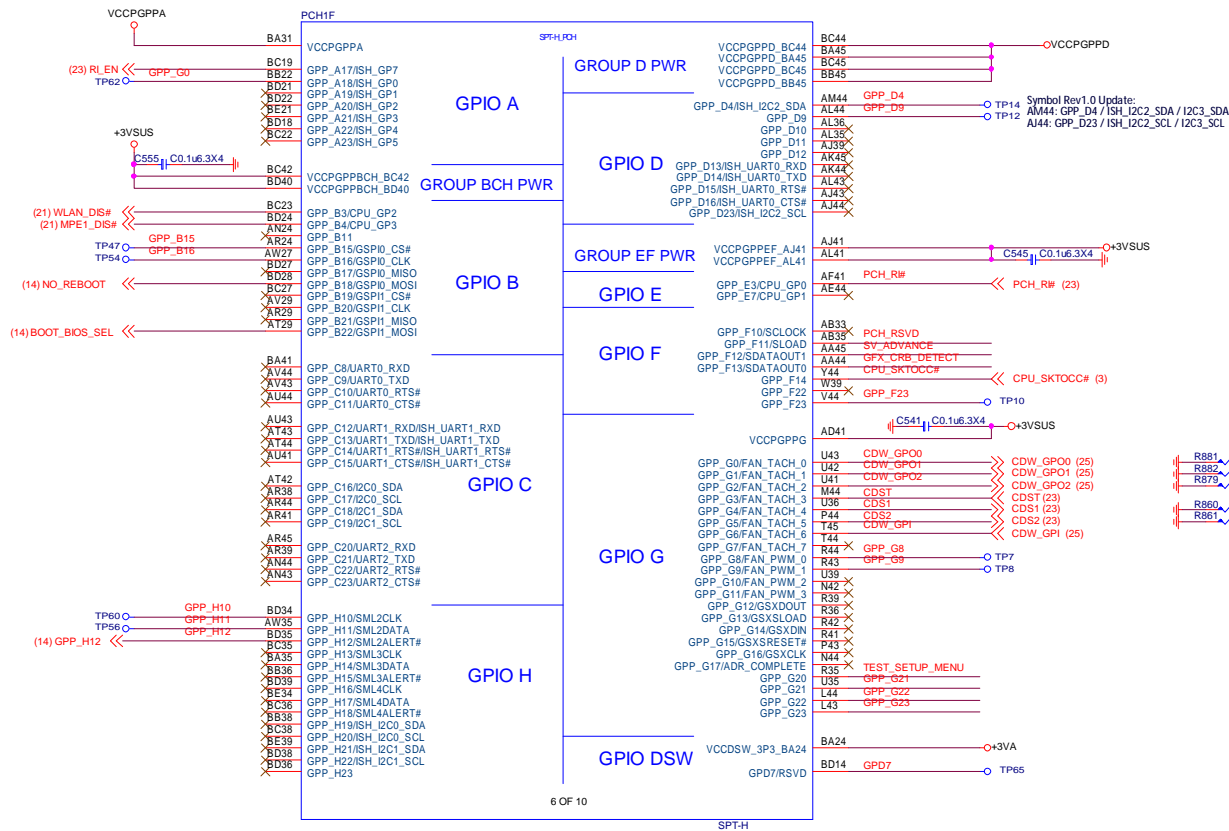
PCH-Clock



PCH-GPIO



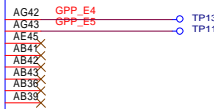
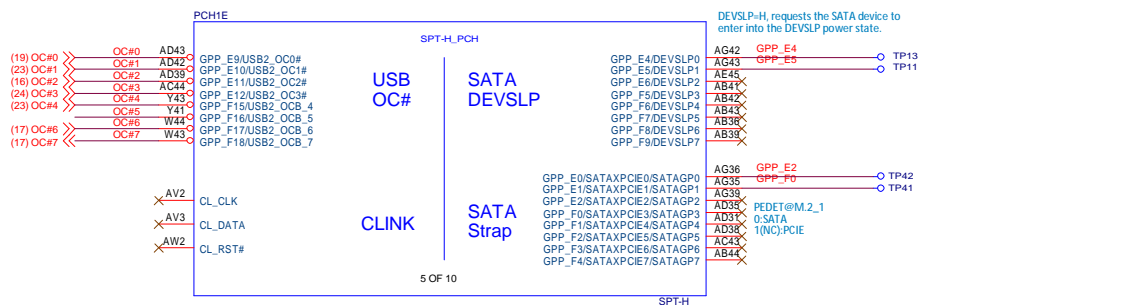
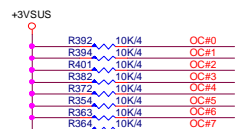
WLAN_DIS# Pull-up to +3V
with 8.2KR @connector
side.
MIPE1_DIS# Pull-up to +3V_TV
with 8.2KR @connector side.



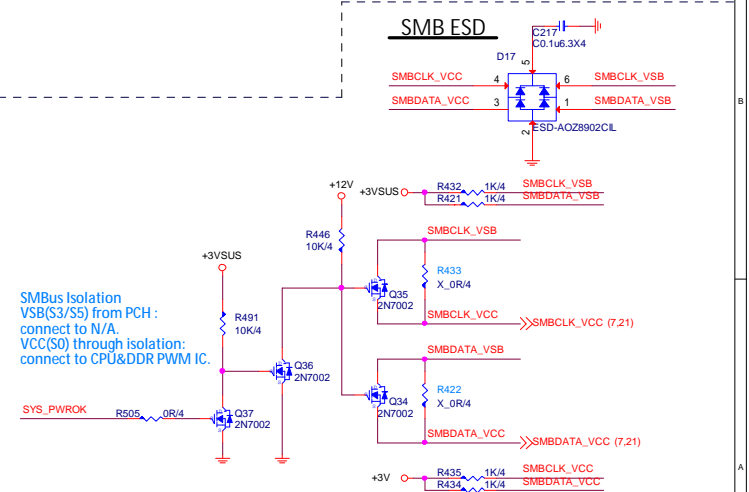
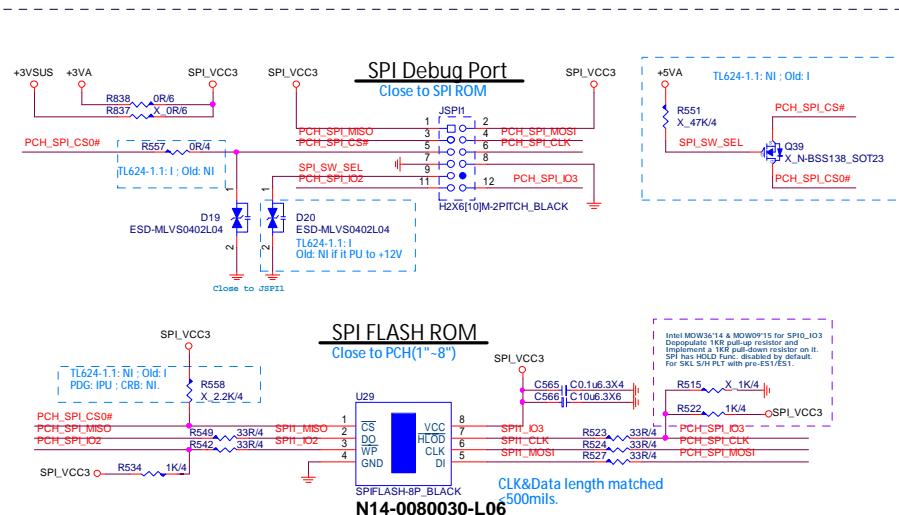
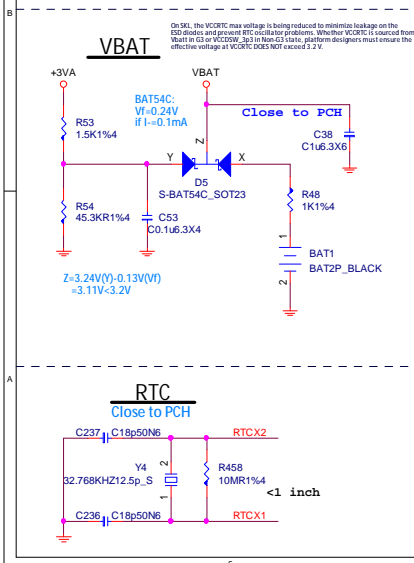
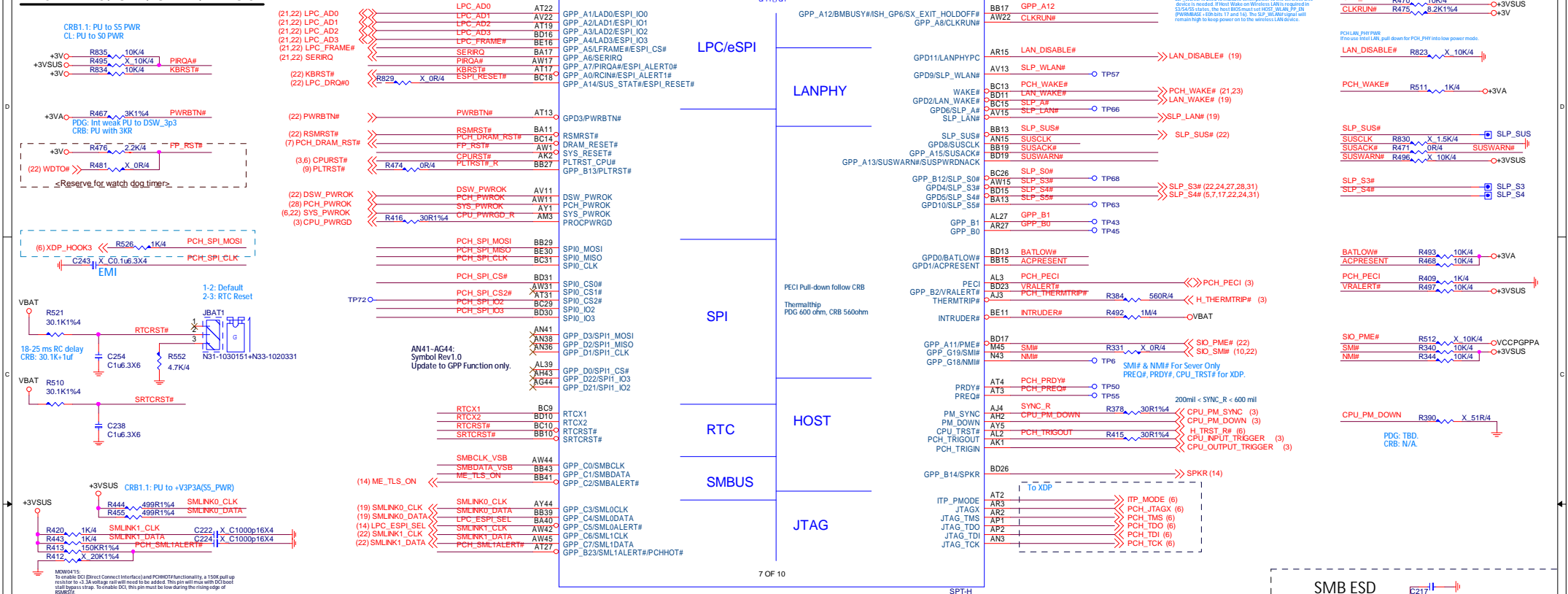
Test Setup Menu
0: Enable
1: Disable



PCH-USB_OC & SATAGP



PCH-LPC/SPI/SMB/MISC



PCH-Power

Power

Current Ratings:

- 6.01A
- 0.03A
- 0.007A
- 0.001A
- 0.001A
- 0.029A
- 0.171A
- 0.204A
- 0.075A
- 0.045A
- 0.348A
- 0.7A
- 0.08A
- 0.036A
- 0.045A

Component List Table:

Symbol	Value	Footprint	Part Number	Manufacturer
C554	1u6.3X4	BA29		
R804	0R/6			
R299	0R/6			
R821	0R/6			
C539	1u6.3X4	AD13		
C567	1u6.3X4	BA22		
C537	1u6.3X4	W15		
C553	1u6.3X4	BA20		
C550	1u6.3X4	AN5		
C207	1u6.3X4			
C522	1u6.3X6	U21		
C524	1u6.3X6			
C514	1u6.3X6	K2		
C513	1u6.3X6			
C517	1u6.3X6	A42		
C519	1u6.3X6			
C548	1u6.3X6	AJ5		
C547	1u6.3X6			

ADVANTECH			
Title: PCH-Power			
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GND

PCH-GND

PCH-Strap

For Strapping pull-up resistor
CRB1.1: 4.7K
PDG2.1: 1-2.2K

Top Swap(SPKR/GPP_B14)



This signal has an integrated weak pull-down resistor (20 K Ω nominal) to disable Top-Block Sway by default.
To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 K Ω \pm 5% resistor.

No Reboot(GSPI0_MOSI/GPP_B18)



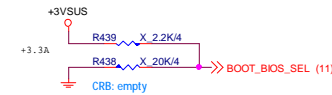
This signal has an integrated weak pull-down resistor (20 K Ω nominal) to disable the no reboot strap functionality by default.
To enable no reboot on TCO Timer expiration, this signal should be pulled-up to V3.3S through a 1k to 2.2 K Ω \pm 5% resistor.

Intel ME Crypto Transport Layer Security (TLS-SMBALERT#/GPP_C2)



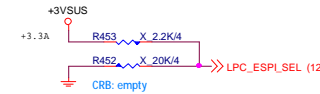
This signal has an integrated weak pull-down resistor (20 K Ω nominal) to disable IntelR ME Cryptographic Transport Layer Security (TLS) cipher suite (no confidentiality).
To enable IntelR ME Cryptographic Transport Layer Security (TLS) cipher suite with confidentiality, this signal should be pulled up to V3.3A through a 1k to 2.2 K Ω \pm 5% resistor.

Boot BIOS Strap Bit (GSP11_MOSI/GPP_B22)



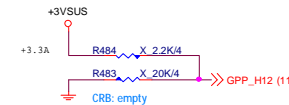
This signal has an integrated weak pull-down resistor (20 K Ω nominal) to default boot from SPI. To enable boot to LPC, this signal should be pulled up to V3.3S through a 1k to 2.2 K Ω \pm 5% resistor.

ESPI/LPC SEL Strap(SMLOALERT#/GPP_C5)



This signal has a weak internal pull-down.
0 = LPC is selected for EC. (Default)
1 = eSPI is selected for EC.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

ESPI Flash Sharing Mode(GPP_H12)



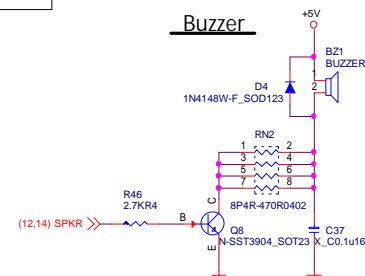
This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
Note: The pull-down resistor is disabled after RSMRST# de-asserts

SPIO_MOSI & SPIO_MISO:
This signal has an internal pull-up.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling(RSMRST#).

SML1ALERT# /PCHHOT#/GPP_B23:
This signal has an internal pull-down.
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling(RSMRST#).

SPIO_IO2 & SPIO_IO3:
This signal has an internal pull-up.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling(RSMRST#).

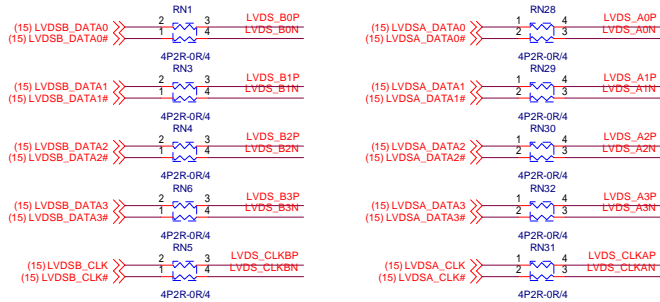
Buzzer



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Title PCH-GND/Strap			
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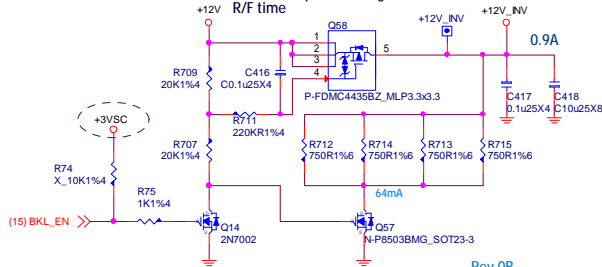
LVDS Output

R3C-000012-W08 Co-layout with L12-9008090-M09
Note: The pin's definition between R&L are difference.

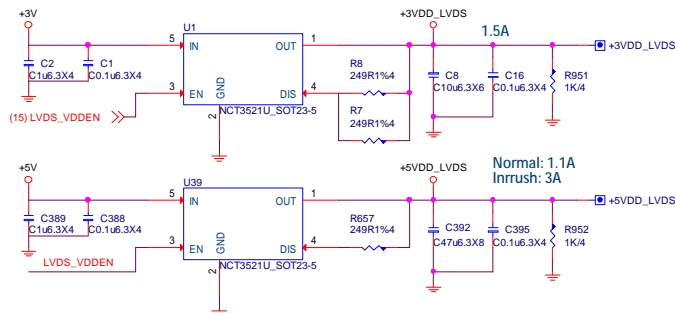


+12V For BL

For 15 inch panel timing and R/F time

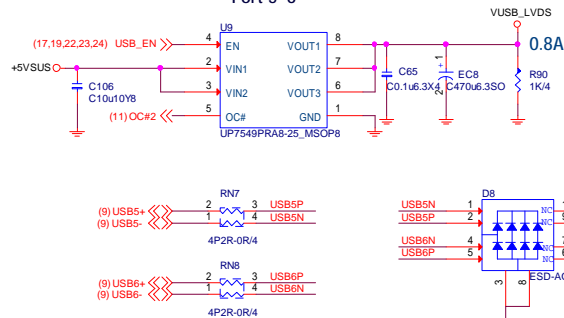


+3V&+5V For LVDS

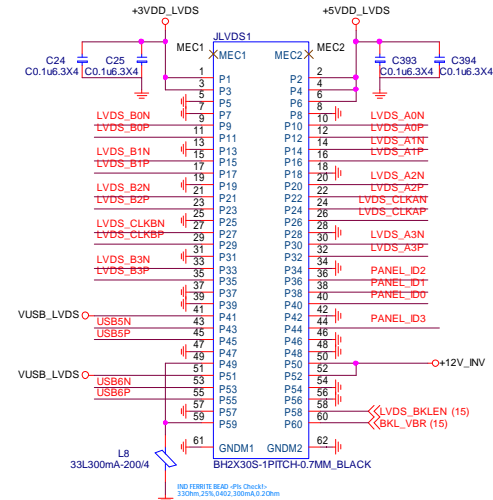


USB Signal & PWR For LVDS Conn.

Port 5-6

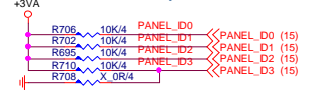


LVDS & BL & USB2.0*2 Conn.



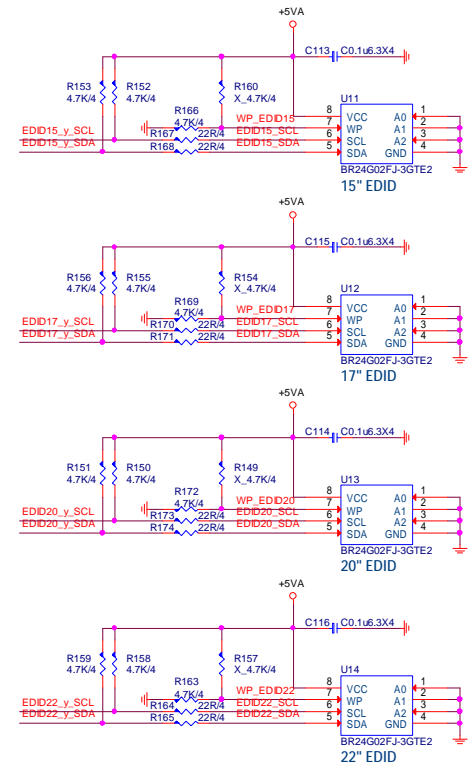
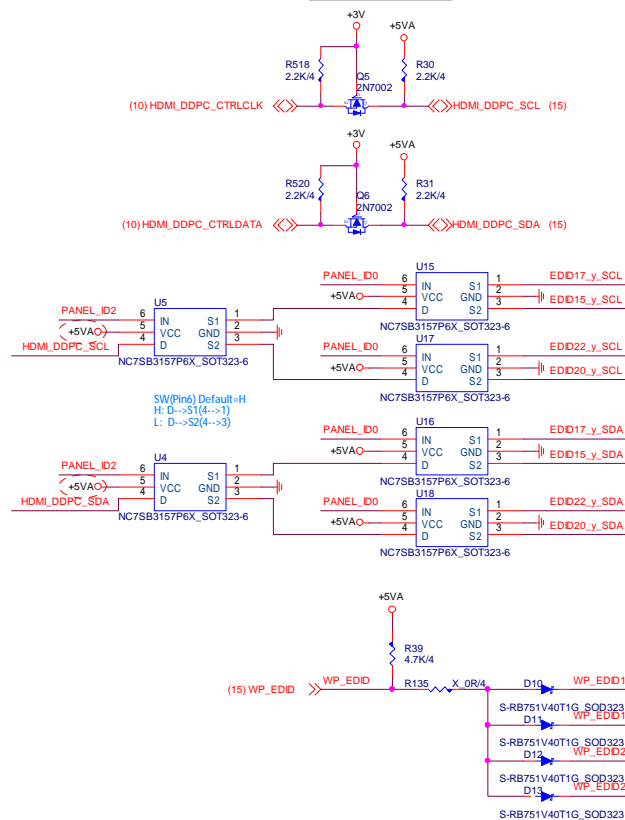
Pannel ID

Panel ID 0-3 controlled by LVDS cable.



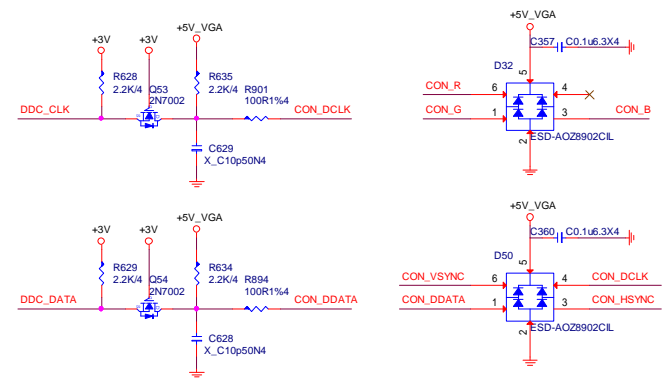
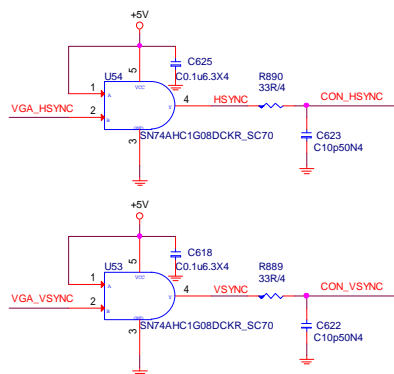
170109
ID 0-2 PD to GND by LVDS cable for 20" monitor.

EDID Switch

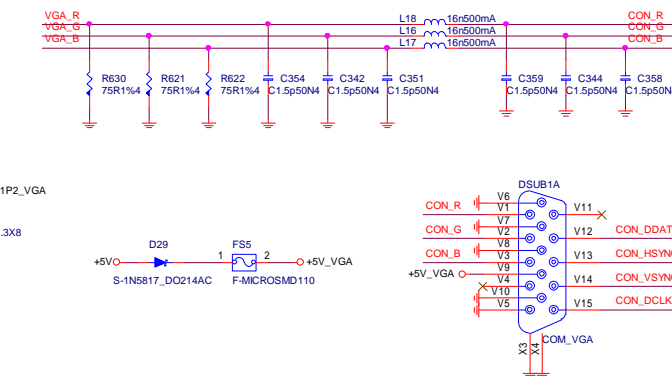


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Title	LVDS Output & EDID Switch & USB2.0*2		
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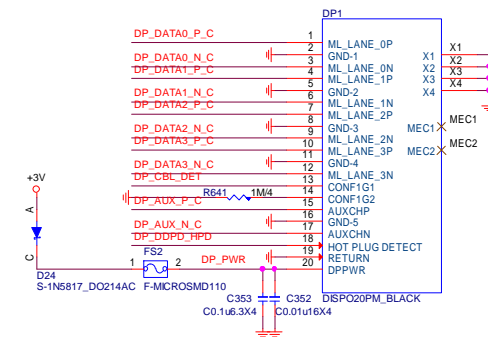
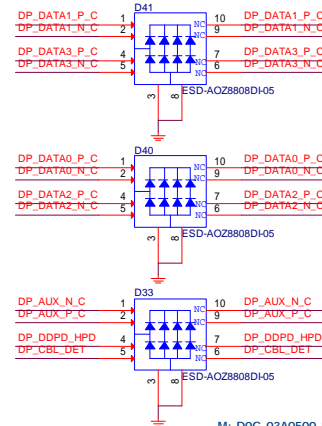
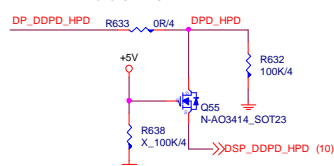
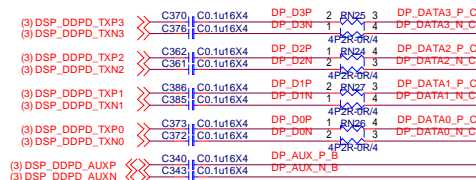
Date: Friday, March 31, 2017 Sheet 17 of 35



$V_{OUT} = VREF \times (R1+R2)/R1$
 $= 0.8 \times (20+10)/20 = 1.2V$

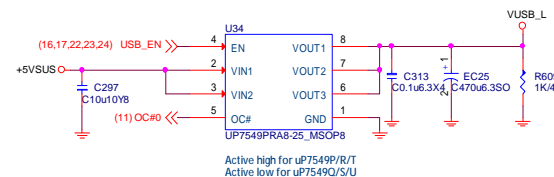
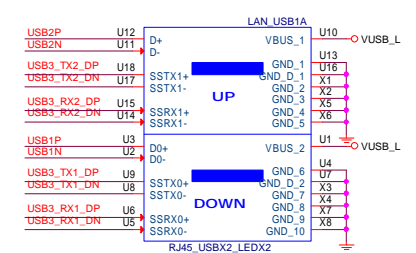
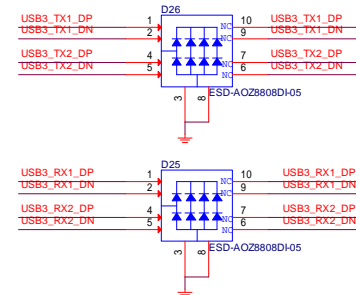
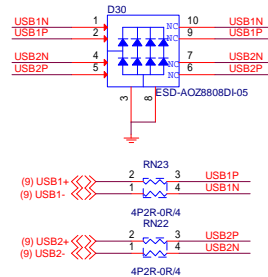
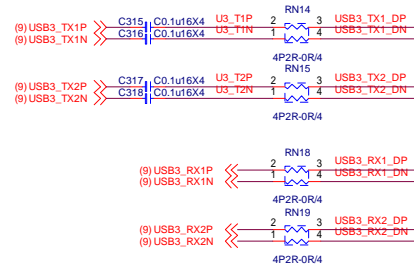
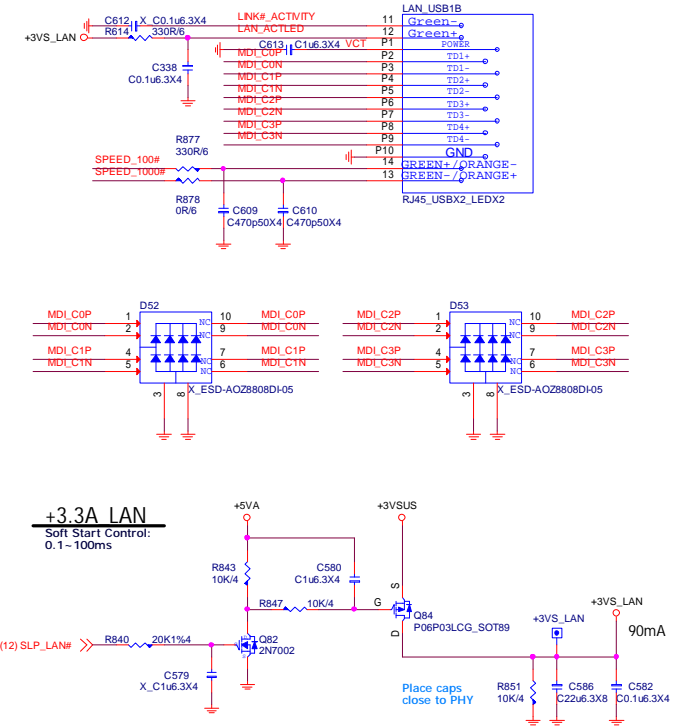
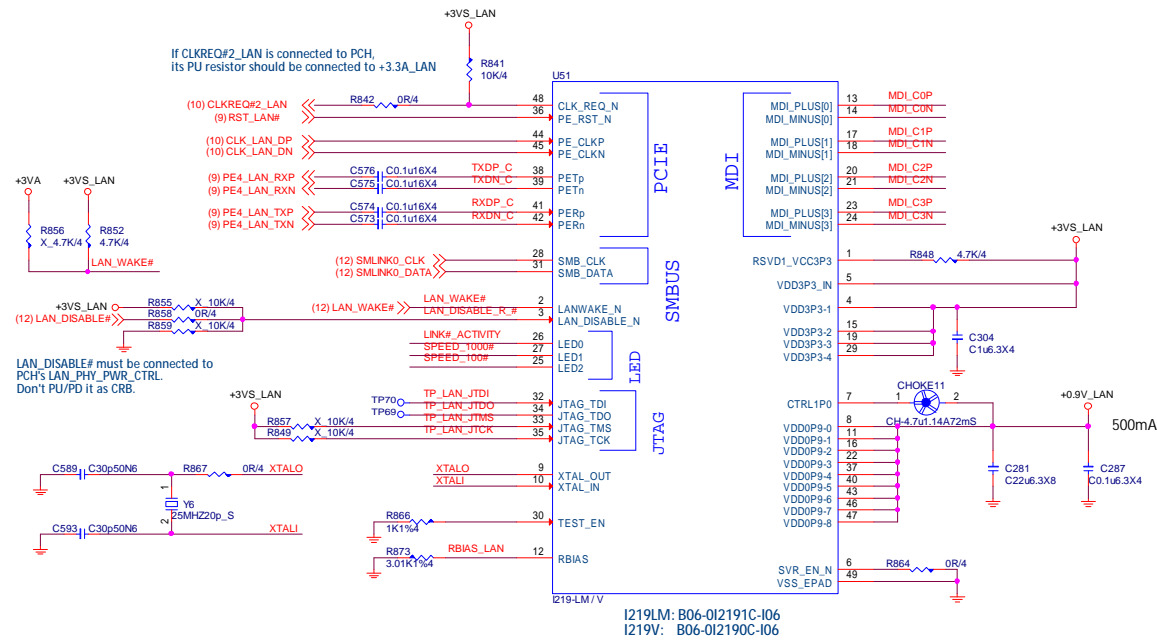


DisplayPort Auxiliary Channel Dual Mode Support Protection Circuit



M: DOG-03A0500-N52
S: DOG-06A050C-A68
S: DOG-05A0300-I14

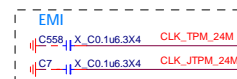
Intel LAN I219-V/LM



Full size (No.19)

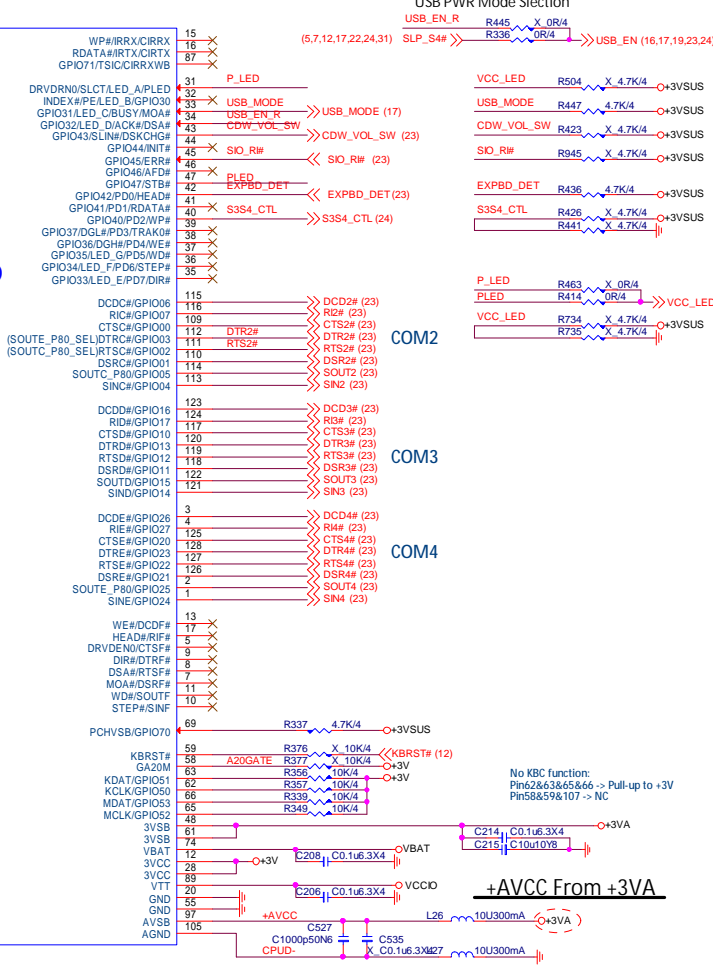
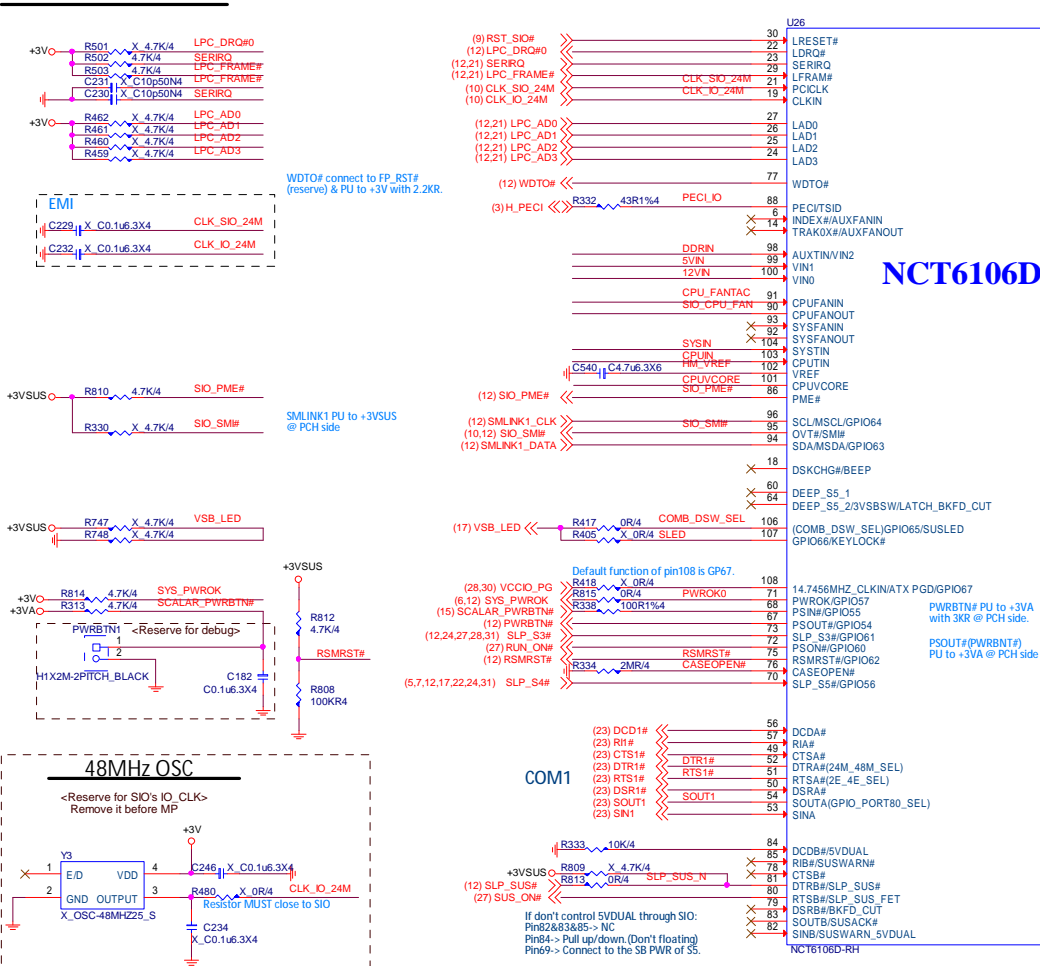


Standard (No.13)

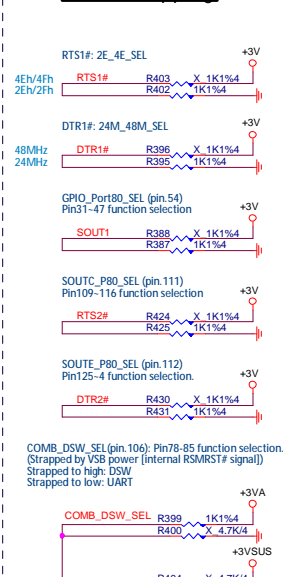


			
Title Mini PCI-E & TPM & JTPM/JLPC & USB2.0*1			
Size	Document Number		Rev
	DMS-SA30		10
Date:	Friday, March 31, 2017	Sheet	21 of 35

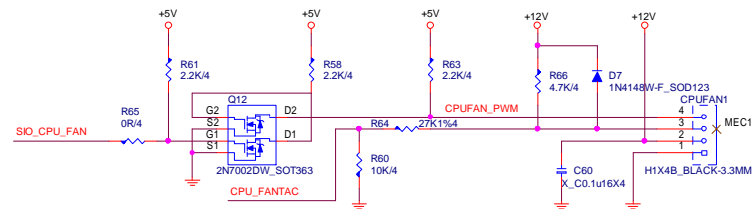
SIO - NCT6106D



H/W Strapping



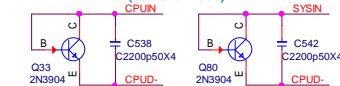
CPU FAN (PWM Mode)



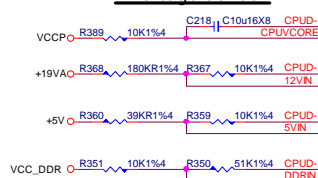
Temperature Sense

Place inner CPU socket &

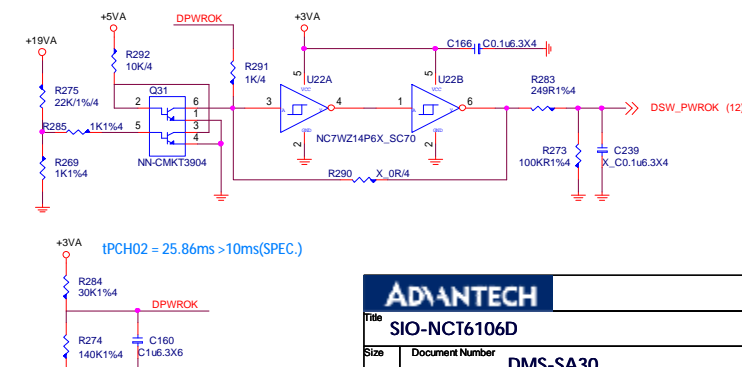
(Current Mode)



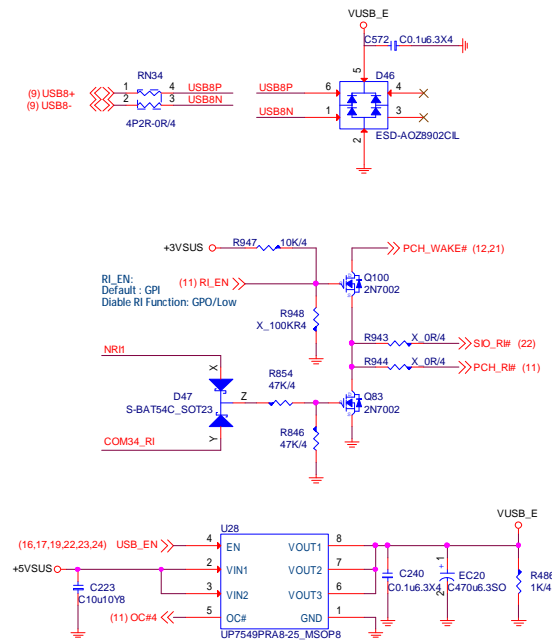
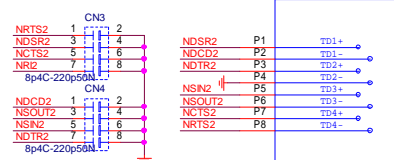
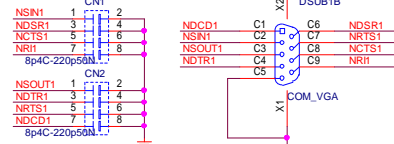
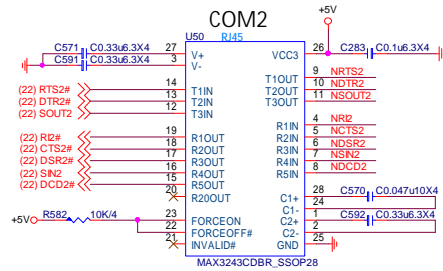
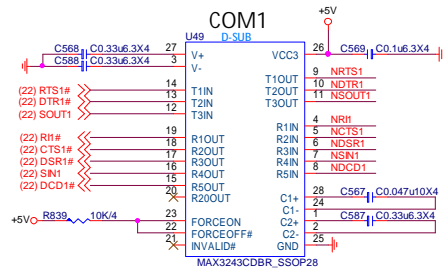
Voltage Sense

DSW PWROK

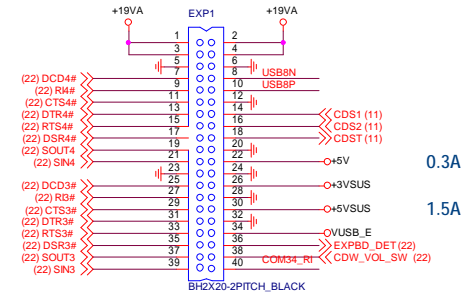
tPCH07 & tPCH14



COM 1&2 MAX3243CDBR



Expansion BD Conn. COM3&4

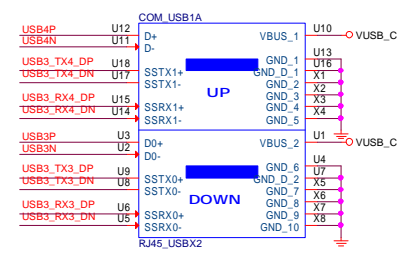
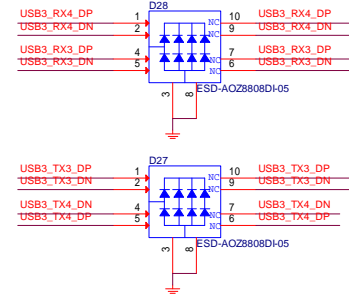
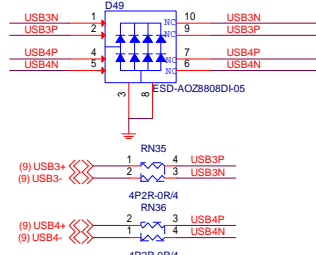
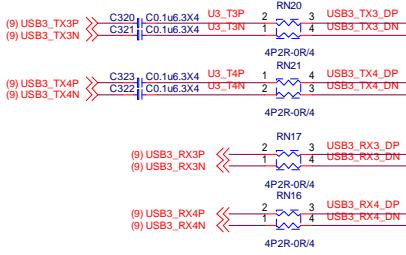


CDS1 & CDS2 :
Cash drawer GPIO output to expansion BD.
Default=Low, this GPIO controlled by AP.

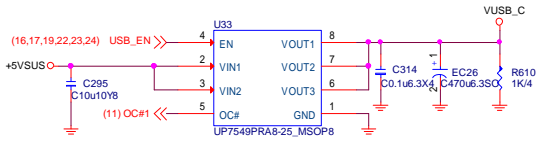
CDST :
Cash drawer status input from expansion BD.
Default=H (Drawer open=Low ; close=High)

EXPBD_DET
No Exp. BD = High -> Disable COM3&COM4
Insert Exp. BD = Low -> Enable COM3&COM4

CDW_VOL_SW
+24VSB/+12VSB selection output for expansion BD.
Default=H, it controlled by BIOS setup manual

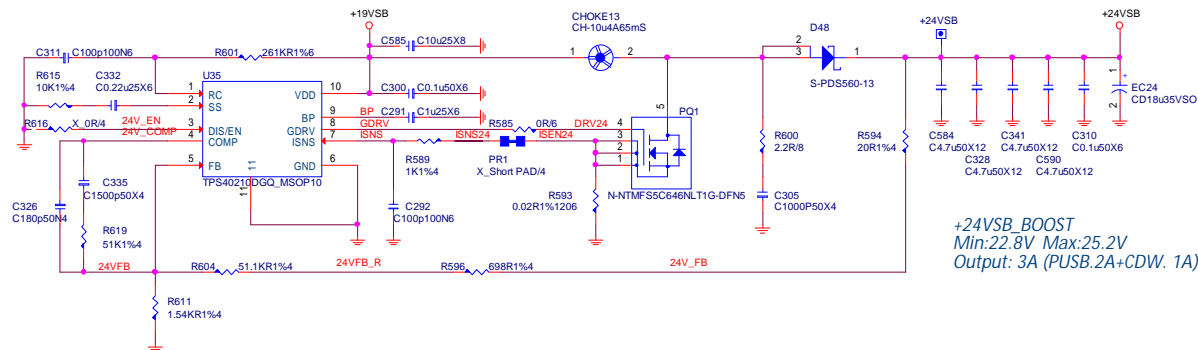
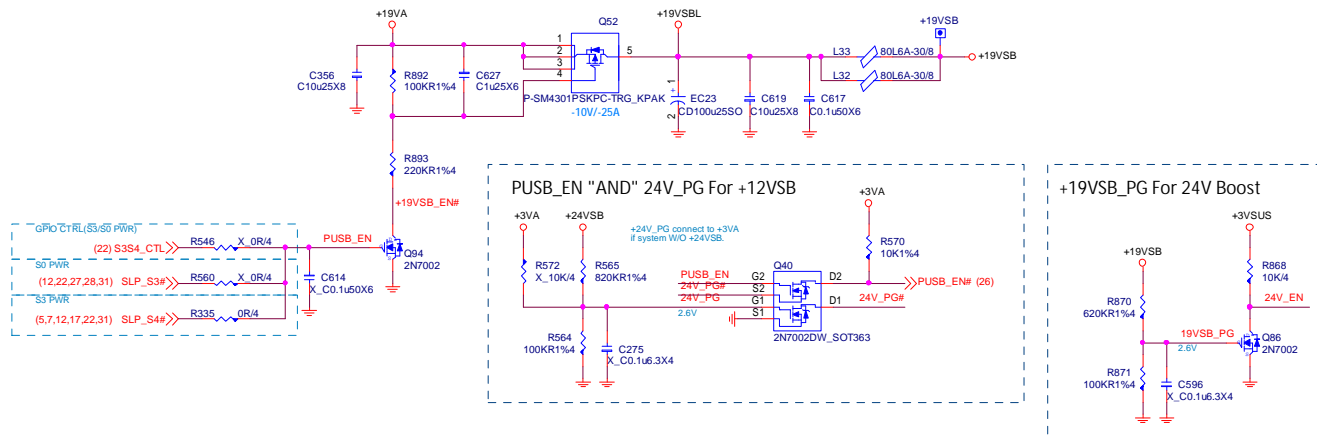


RJ45(COM+USB)
USB3.0: N58-26F0031-S42
USB2.0: N58-16F0291-S42



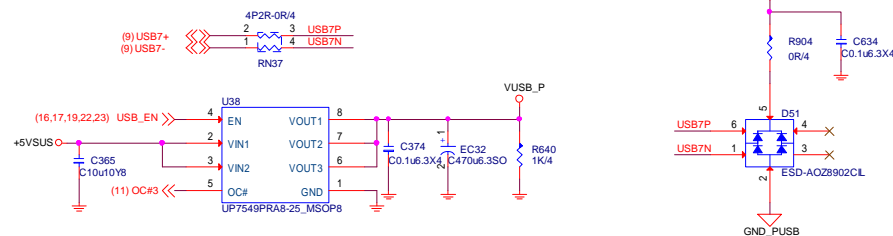
+24V Boost (S3/S0 PWR)

TPS40210

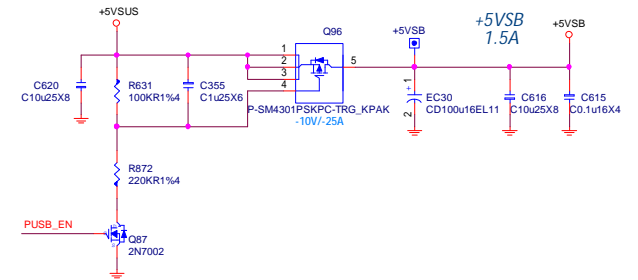


USB Signal & PWR For PWR USB

Port 13

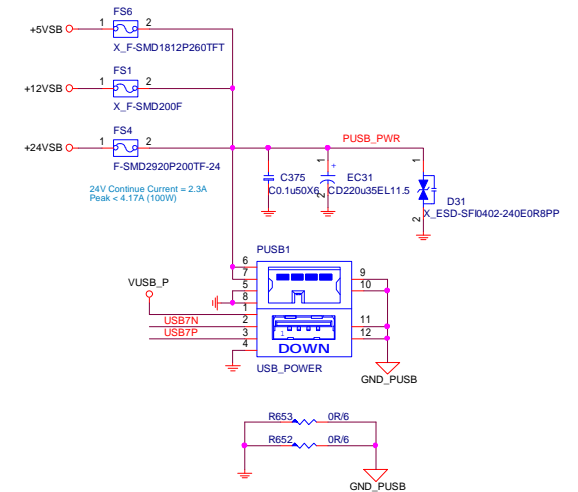


+5VSB (S3/S0 PWR)



Power USB

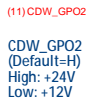
The default spec would stay with +24VUSB spec as VS defined, and reserve the +12V/+5V PUSB EE design on MB for option requirement.



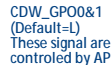
ADVANTECH			
File	+24V Boost & +5VSB & Power USB(U2*1)		
Size	Document Number	DMS-SA30	Rev 10
Date	Friday, March 31, 2017	Sheet 24	of 35

+V CASH PWR Selection

+24VSB / +12VSB



Cash Drawer



Cash drawer status input from RJ11 connector
Default=H (Drawer Open=Low ; Close=High)



Drawer B

Cash Drawer Close

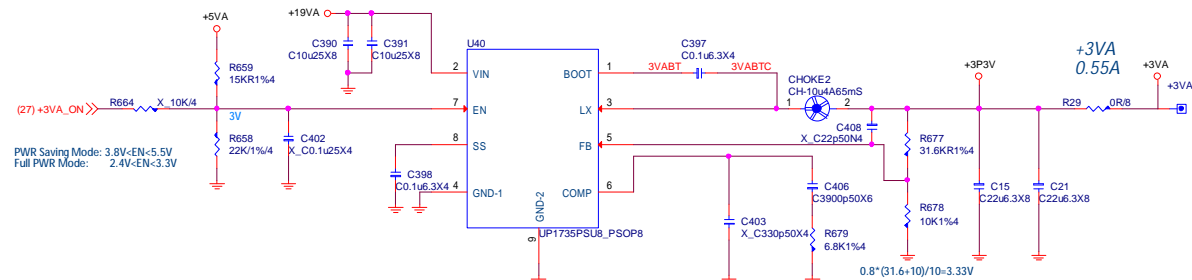
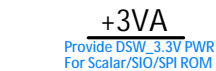
Cash Drawer Open

Title	
Cash Draw	
Size	Document Number

DMS-SA30

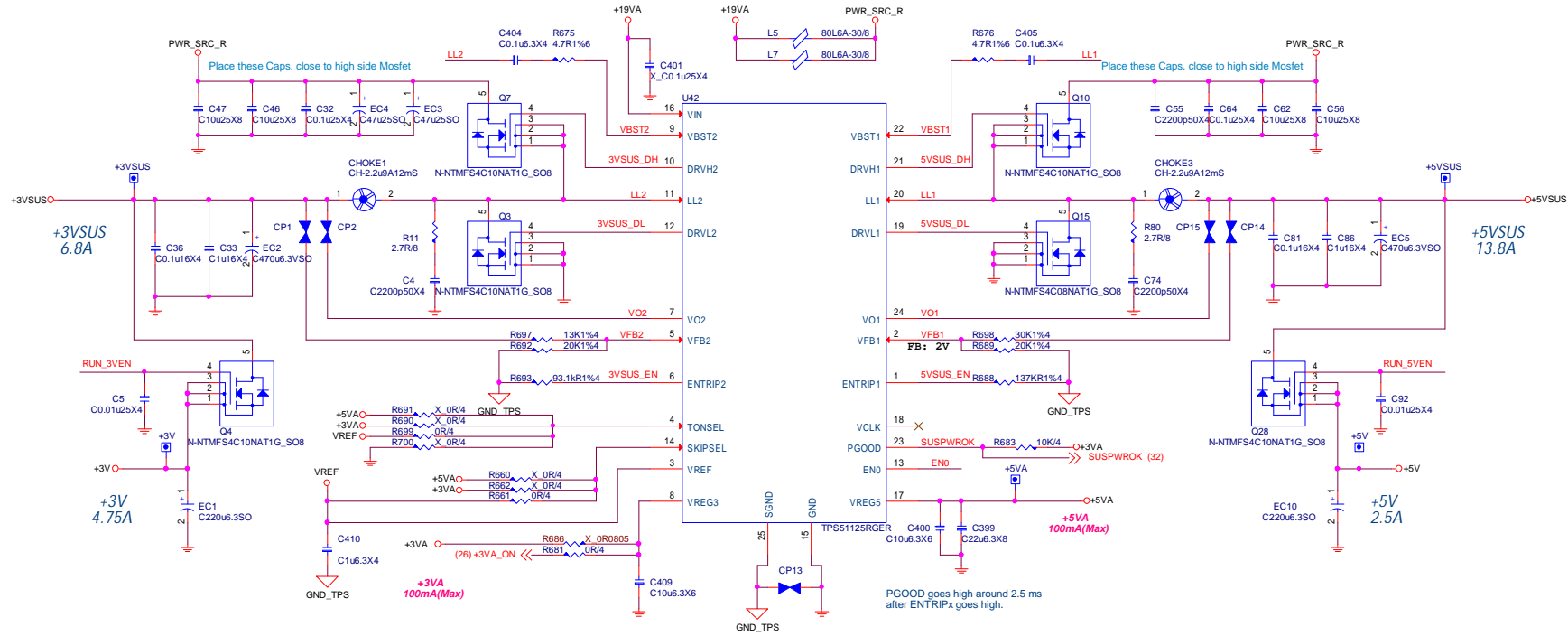
Date: Friday, March 31, 2017 Sheet 25 of 35

+12VSB (S3/S0 PWR)

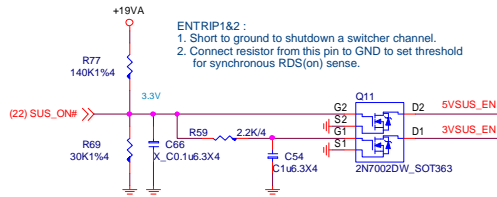


System Power

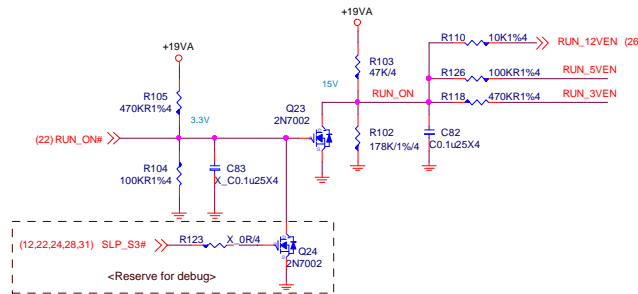
+5VSUS/+3VSUS/+5V/+3V



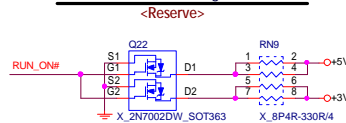
+5VSUS & +3VSUS Enable



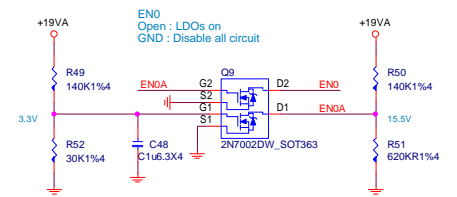
+5V & +3V Enable



+5V & +3V Discharge Circuit



ENO delay to wait PWR_SRC ready



ADIANTECH

System Power

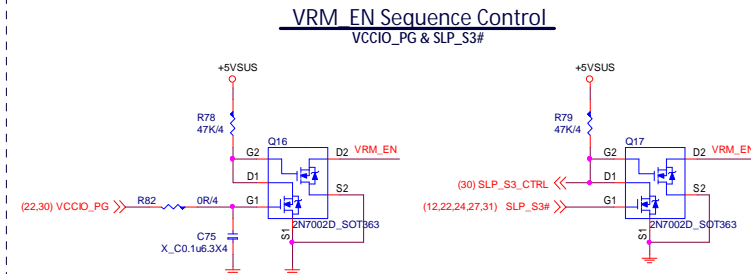
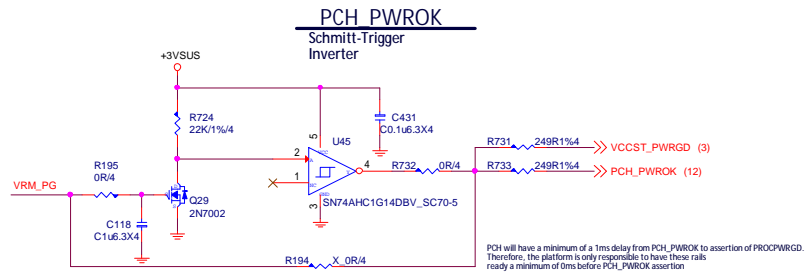
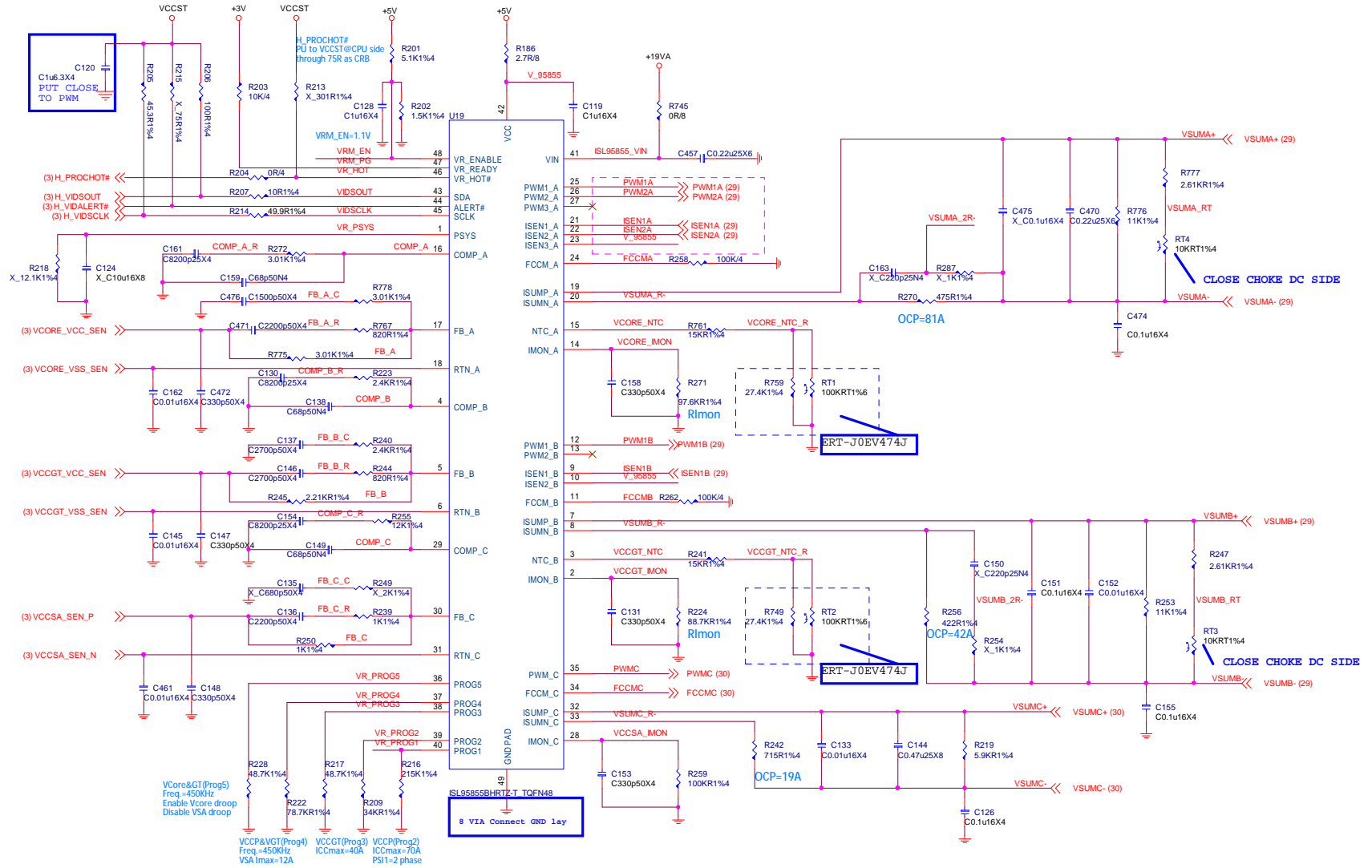
Document Number DMS-SA30

Date: Friday, March 31, 2017

Sheet 27 of 35

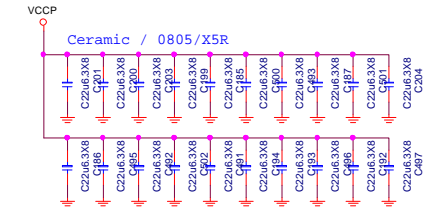
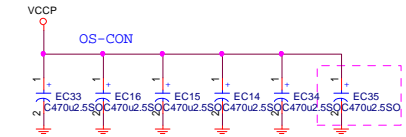
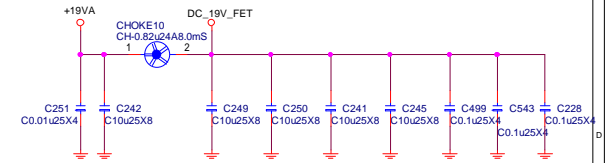
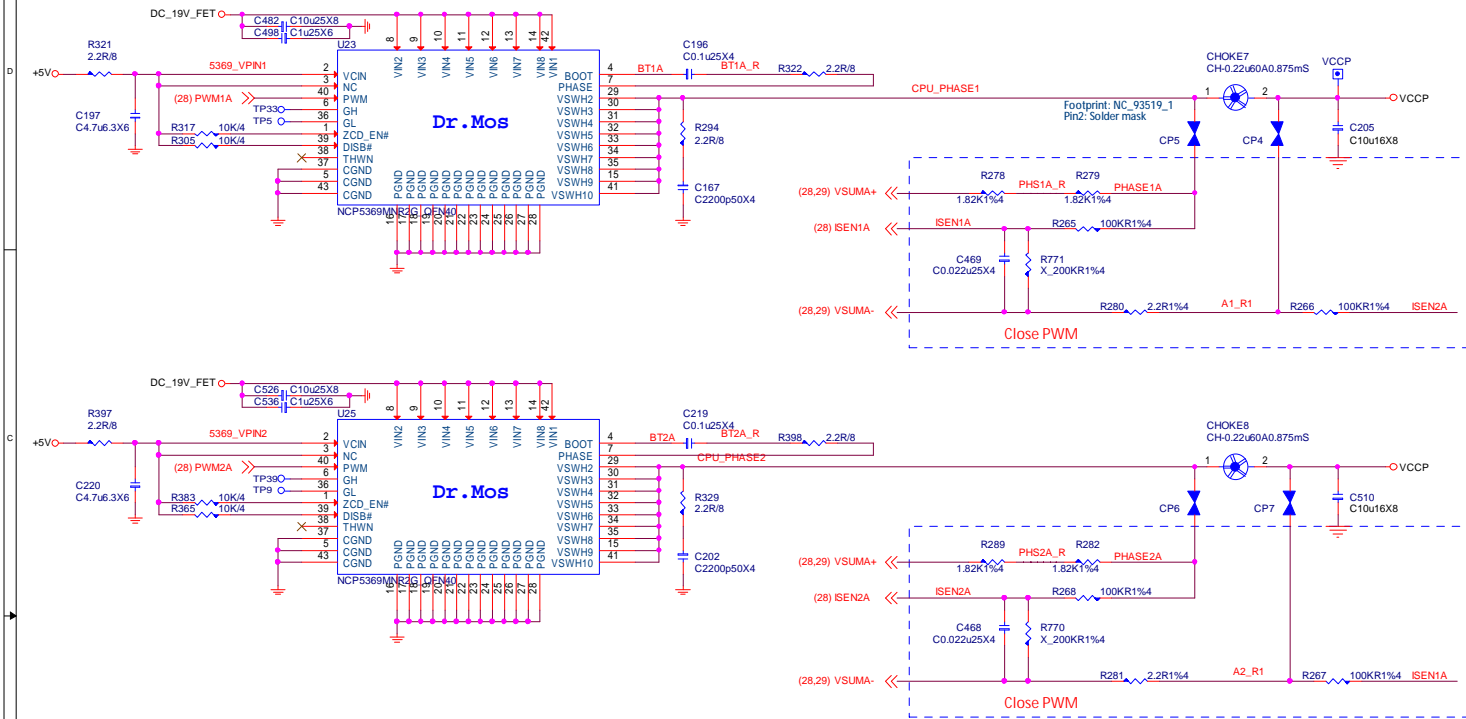
Rev 10

SKL S-line 35W (ISL9585B)



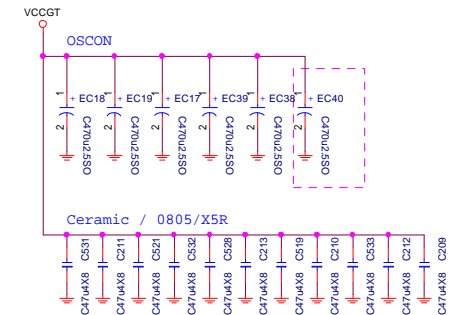
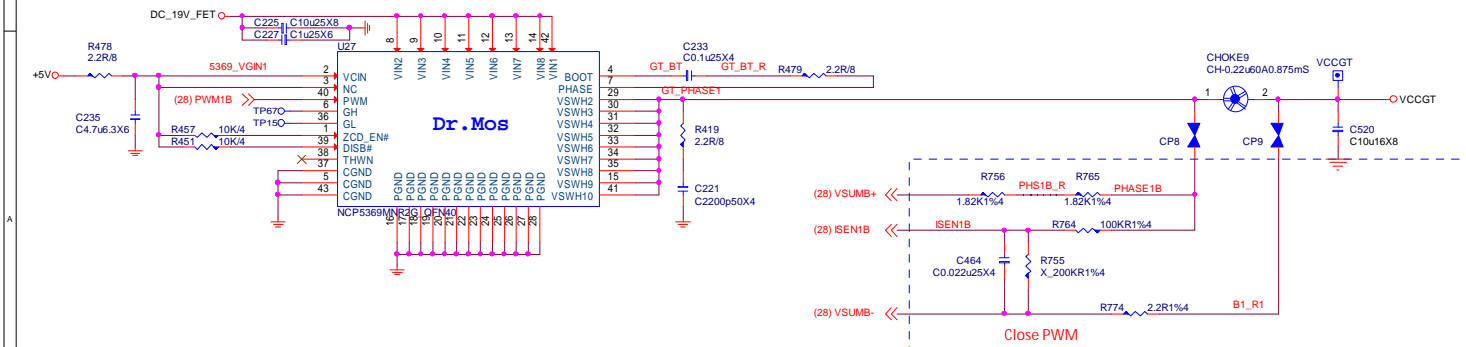
VCCP

0.55V~1.52V output range
TDC=45A
EDC=66A

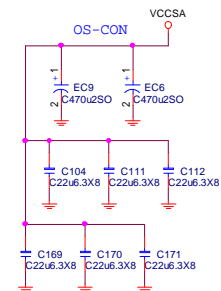
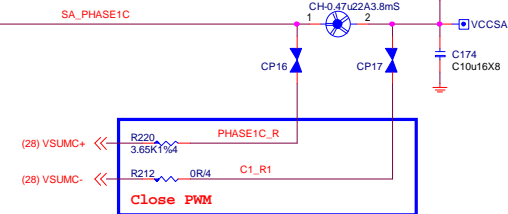
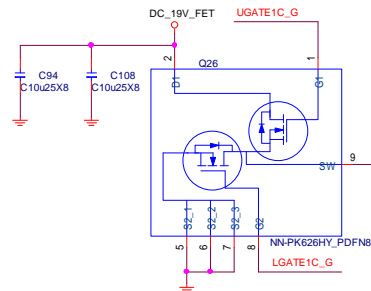
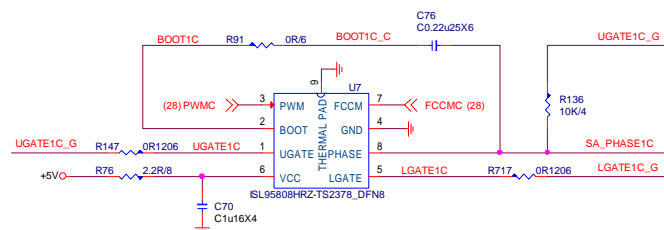


VCCGT

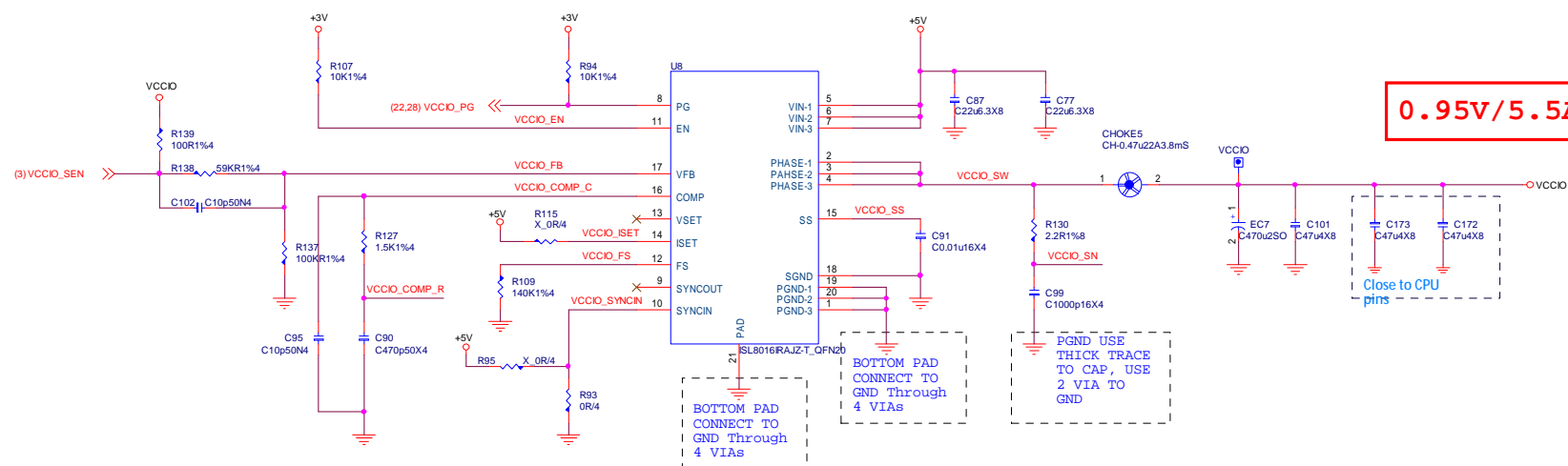
0.55V~1.5V output range
TDC=25A
EDC=35A



VCCSA

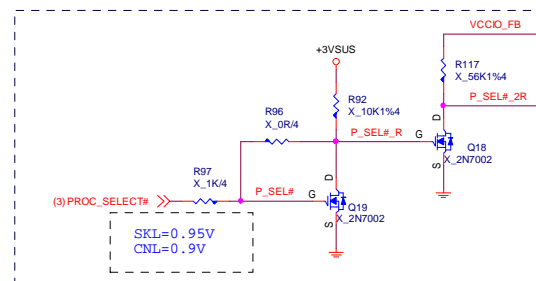
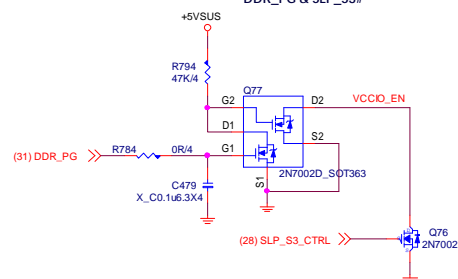


1.05V/11.1A

VCCIO

0.95V/5.5A

VCCIO EN Sequence Control



VCC_DDR

The schematic diagram illustrates the power plane for the VCC_DDR, showing the connection of the I32-1589L0C-005 chip to the DDR memory modules. The diagram includes the following components and connections:

- Power Supply Rails:** +5VUS, +3VUS, +3V, +19VA, and VCC_DDR_VIN.
- Decoupling Capacitors:** C530 (C1u16X4), C525 (C0.1u6.3X4), C544 (C0.1u6.3X4), C564 (C0.12u5X4), C560 (C10u25X8), C562 (C10u25X8), C559 (C10u25X8), C511 (C22p50N4), C509 (C0.1u6.3X4), C507 (C0.01u16X4), C508 (C6800p16X4), C506 (C6800p16X4).
- Resistors:** R803 (10K1%4), R802 (X_10K1%4), R800 (5.1K1%4), R799 (2K1%4), R801 (X_13K1%4), R816 (2.2R/8), R820 (2.2R1%8), R833 (2.2R/8), R831 (10K/4), R832 (0R/8), R819 (5.36KR1%4), R796 (0R/4), R797 (1K1%4), R795 (1.07KR1%4).
- DDR Memory Module (U48):** NCP1589LMNTWG_DFN10, I32-1589L0C-005. Pins include PGOOD, COMP, EN, LG, FB, SEN, RC, FB, RC.
- Callout Box:** BOTTOM PAD CONNECT TO GND Through 6 VIAS.
- Other Components:** D45 (S-BAT54C, SOT23), C546 (C0.22u25X6), L29 (30L6A-10/8), L28 (30L6A-10/8), O81 (NN-FDMS3669S_POWER56-8), R836 (2.2R/8), C563 (C220p50X4).

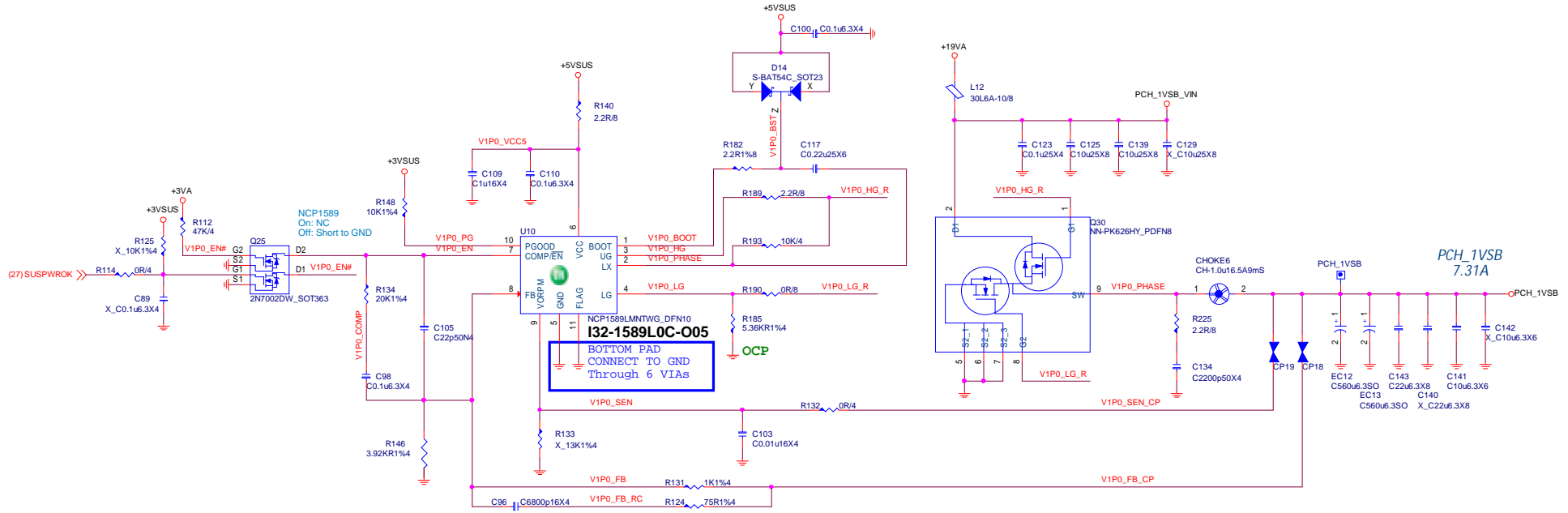
I9C-1727P0C-U33

CONNECT TO GND PLANE BY 4 VIAs

$V_{out} = 0.6 \cdot (R1 + R2) / R2 = 0.6 \cdot (31.6K + 10K) / 10K = 2.49V$

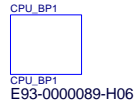
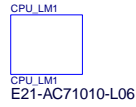
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PCH_1VSB



CPU Socket

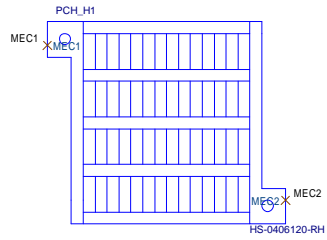
ILM + BP



PCB



PCH Heatsink



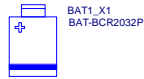
SPI ROM



BIOS Label



Battery



Option Parts

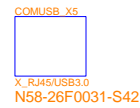
PCH Option



LAN Chip Option



COM_USB1 Option

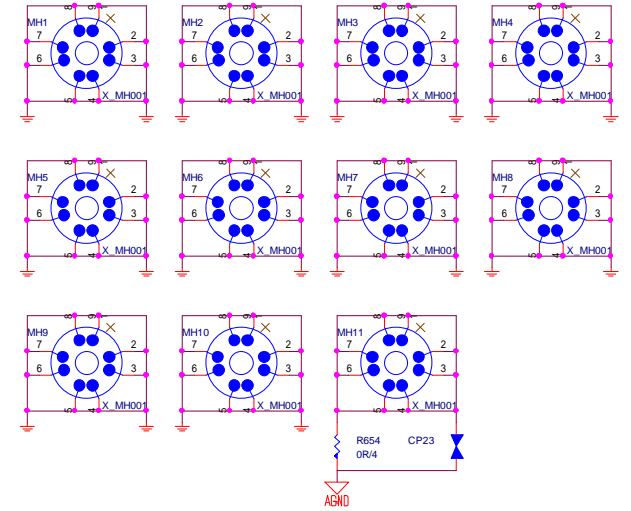


SPI ROM Option

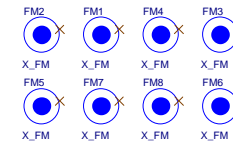


BIOS 8M (H110) : M31-25Q6443-W03
BIOS 16M (H170/Q170) :
M31-2512832-M24 & M31-2512893-W03

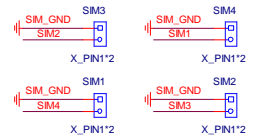
Mounting Holes



Optical Fiducial Marks-120

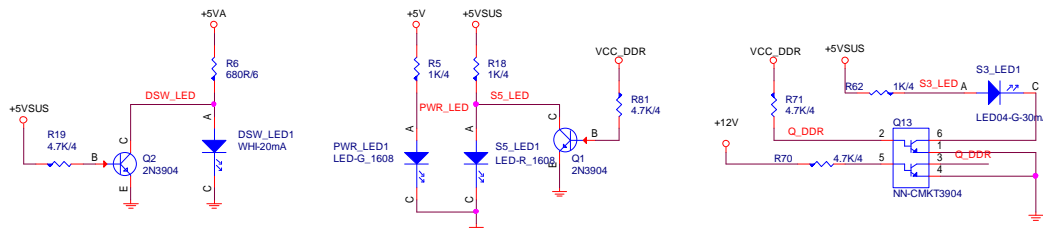


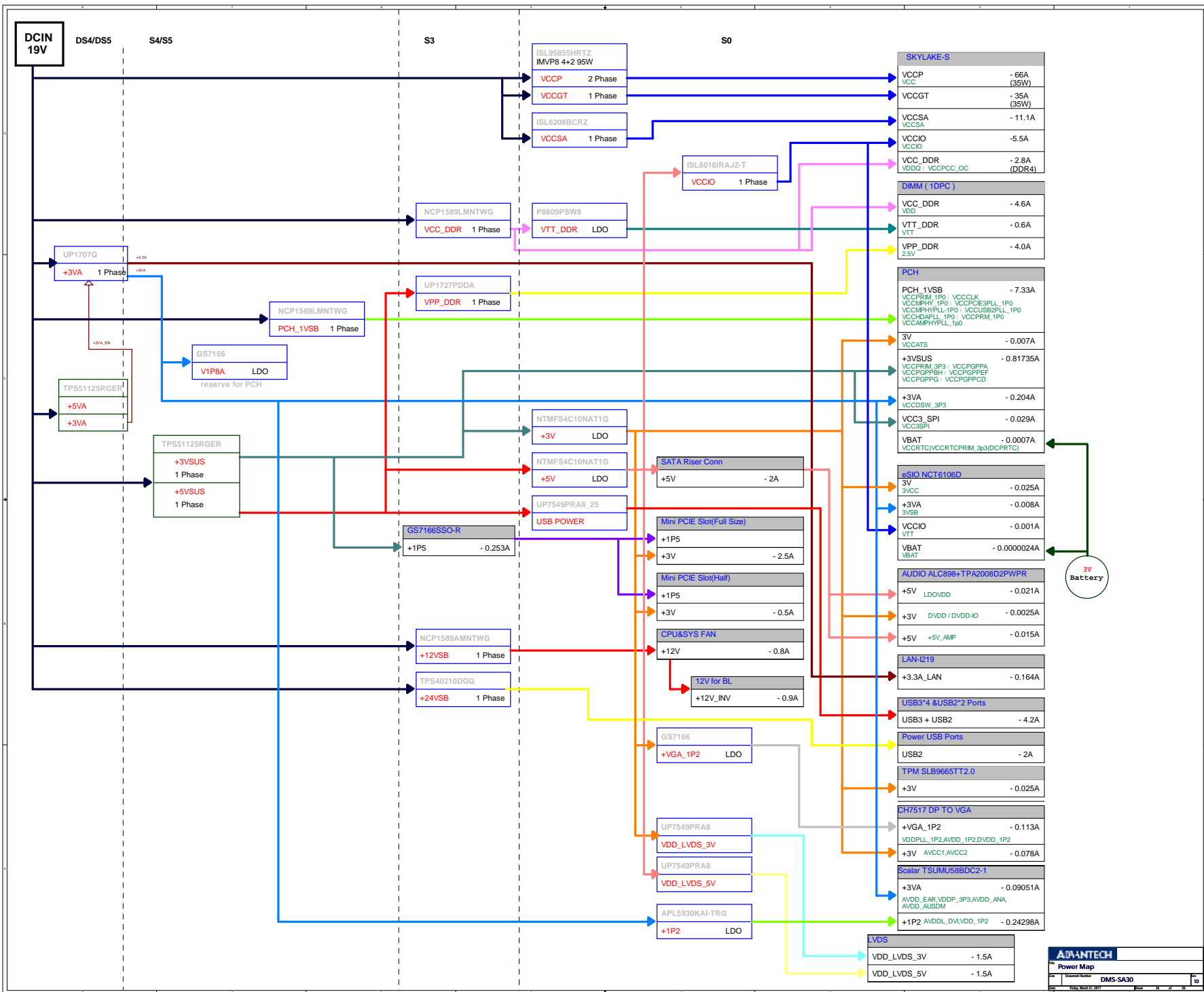
Simulation



Power status LEDs

<Debug only, remove it before MP>





DMS-SA30 Rev.0A : (161226)
DMS-SA30 Rev.0B : (170313)

Page 3:
* The connection of CH7517 (VGA) change from eDP(Port-A) to DP(Port-B) to prevent some limitation of eDP.
Page 5:
* Reserved SLP_S4_CTL from Q59.D1 for the option of turn on timing of +12VSB&+12V.
Page 9:
* Reserve R925 (RST_GL850#) for GL-850 USB HUB.
* Change/Swap configuration of USB2.0 Port 7~14.
* SATA connection change from SATA2B&3B to SATA0B&1B to same as the display of DMS-SA20's BIOS Setup Manual.
Page 10:
* C195 change from 22P50N4 to 12P50N6 and C189 change from 22P50N4 to 15P50N6 by crystal matching test report.
Page 11:
* Change/Swap configuration of USB2.0 OC#3~7.
* No stuff the pull up resistor R391 of PCH_RI# because this function change to SIO by BIOS request.
Page 12:
* C236&C237 change from 12P50N6 to 18P50N6 by crystal matching test report.
* R54 change from 78.7K1%4 to 45.3K1%4 to same as CRB design.
Page 15:
* Y1 change from 14.318M20P(D04-0103000-F07) to 14.318M12P(D04-0103700-F07) by crystal matching test report.
* No stuff D9 and stuff R129 to solve noise from BKL_VBR.(170322)
Page 16:
* C392 change from 10uf6.3X6 to 47u6.3X8 for the inrush current of +5VDD_LVDS.
* C16&C392 stuff 1KR4 to discharge *VDD_LVDS under G3.(170322)
Page 17:
* Add R907~R911 for the gates of Q66~Q70 to prevent gate floating problem.
* Add U55 (GL850 USB2.0 HUB) and related components for H110 Sku.
* Remove RN10~13 ; Add R935~942 for Q170 Sku.
Page 18:
* The connection of CH7517 (VGA) change from eDP (Port-A) to DP (Port-B) to prevent some limitation of eDP.
* F/W version of CH7517 change from 3.1.0.7 (B07-7517A1C-C25) to B000.05.01.13 (B07-7517A4C-C25).
* C298&C298 change from 18P50N4 to 15P50N6 by crystal matching test report.
* Swap D32&D50's connection by layout request.
* L16~L18 change from 82nf300mA to 16nf500mA ; C354/C342/C351/C359/C344/C358 change from 10pf50N4 to 1.5pf50N4 for R/F time and Over/Under shoot adjustment.
Page 19:
* LAN_USB1 change footprint from IOA_RJ45_USB2_LED2_32_1 to IOA_RJ45_USB2_LED2_32.
* C589&C593 change from 22P50N4 to 30P50N6 by crystal matching test report.
* Reserve D52&D53(ESD diode) by EMI request.
Page 20:
* C325&C312 change from 1u16X4 to 0.1u16X4 because Ci must be 10 times smaller than C-Bypass, the value range of C-Bypass is 0.47uf to 1uf.
* C607 change from 1u16X4(X5R) to 1u25X6(X7R) for low-ESR requirement of BYPASS(pin22).
* Change the power source of L36(LDOVDD) from +5V to +5VSUS for S3 wake up noise issue.
* Reserve L41 to add a power source from +5VSUS for +5V_AMP.
Page 21:
* No stuff R10(SERIRQ) because not support TPM card for JTPM1.
Page 22:
* Reserve a connection(SIO_RI#) between U26.45(GP45) and Q83.D by BIOS request.
* Modify Hardware Monitor(Voltage Sense) of +12V change to +19VA and R368 change from 110K1%4 to 180K1%4.
* No stuff Y3&C246 because it only for defensive design.(170322)
Page 23:
* C567&C570 change from 0.1u6.3X4 to 0.047u10X4 ; C568&C588&C587&C571&C591&C592 change from 0.1u6.3X4 to 0.33u6.3X4 to meet the requirement of MAX3243 datasheet.
* Reserve R943&R944 for the signal of RI# by BIOS request.
* Add Q100 and R947 to change the connection from PCH_GPIO to PCH_WAKE# by BIOS request.
Page 24:
* R593 change from 0.01R1%XTRA to 0.02R1%1206 for OCP adjustment.
* FS4 change from RUEF300K to SMD2920P200-24 for safety.
Page 25:
* FS3 change from FUSE-4A to RLD30P300 to same as EXP BD.
Page 26:
* Remove R650 because without current sense feature.
* Reserved R650 (SLP_S4_CTL) for the option of turn on timing of +12VSB&+12V.
* EC22 change from 220uf/16V/Solid DIP (C71-2211610-N07) to 100uf/16V/Solid SMD (C71-1011680-N07) for ME limitation.
* EC21 change from 100uf/16V/EL_DIP (C94-1011621-N07) to 100uf/16V/Solid SMD (C71-1011680-N07) for ME limitation.
* C274 change from 0.047uf10X4 to 0.1uf25X4 & C266 stuff 470pf50X4 & R559 stuff 75R1%4 12V_COMP&FB.
Page 27:
* R51 change from 30K1% to 620K1% to solve +3VA&+5VA abnormal turn on issue.
* The pulled-up PWR source of SUS_ON# change from +3VA to +19VA and R77 change from 10K1% to 140K1% and R69 change from 100K1% to 30K1% to solve +3VSUS&+5VSUS abnormal turn on issue.
Page 28:
* No stuff C475 and C470 change from 0.1uf16X4 to 0.22uf25X6 for ISUM_A.
* C152 change from 0.012uf16X4 to 0.01uf16X4 for ISUM_B.
* R224 change from 93.1KR1% to 88.7KR1% for I-mon.
* R242 change from 1.54K1% to 715R1% to adjust OCP=19A.
* C137 change from 2200pf50X4 to 2700pf50X4 and R245 change from 2.4KR1% to 2.1KR1% for FB_B.
Page 31:
* R800 change from 20KR1% to 5.1KR1% for DDR_COMP.
* Add R926 (10R1%6) and modify circuit to same as the demo circuit of UP1727 (U47)'s datasheet.
Page 33:
* PCB1 change from Rev.0A(P30-07B010A-E48) to Rev.0B(P30-07B010B-E48).
* Remove R651 and change it to CP23(copper) by process request.

Others:
* D20&D37&D38&D42&D43 change from DOG-2950500-SIO to DOG-2710510-I05 by purchase request.
* C190&C216&C464&C468&C469 change from 0.22uf16X4 (C11-2232022-W08) to 0.22uf25X4 (C11-2232022-W08) by purchase request.
* C146 change from 2700pf25X4 (C11-2722022-W08) to 2700pf50X4 (C11-2722822-W08/C11-2722012-S02) by purchase request.
* BIOS_X3 change from W25Q64FVSSIQ (M31-25Q6443-W03) to W25Q64JVSSIQ (M31-25Q6443-W03) by purchase request.
* All of the net name of PWR_SRC change to +19VA.

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Page 6:
* Stuff R143&R144&R145 by schematic checklist of XDP.
Page 10:
* DDPC_CTRLDATE pull up to +3V through R949(2.2KR4) to enable DDI Port- B and reserve TP71.
* Add R950 to disable DDI Port-A(eDP).
* R509 change from 10KR4 to 100KR4 for DDPD_HPD3.
Page 12:
* No stuff R551 for TL-624-1.1.
* Add TP72 (PCH_SPL_CS2#) for debug.
Page 16:
* Add discharge resistors R951&R952(1KR4) for +3VDD&+5VDD_LVDS power plane.
* C16&C392 stuff 0.1uf6.3X4.
Page 22:
* No stuff R330 because no SMI# requirement.
Page 33:
* PCB1 change from Rev.0B(P30-07B010B-E48) to Rev.10(P30-07B0110-E48).

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